DEVELOPMENT OF NEW CHARACTERIZATION TECHNIQUES FOR THIN-FILM SILICON-ON-INSULATOR (SOI) MATERIALS AND DEVICES

BY

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Abstract of Dissertation Presented to the Graduate School
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DEVELOPMENT OF NEW CHARACTERIZATION TECHNIQUES FOR THIN-FILM SILICON-ON-INSULATOR (SOI) MATERIALS AND DEVICES

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This research effort mainly deals with the development of new electrical and optical characterization techniques and the modeling of thin-film silicon-on-insulator (SOI) materials and devices for VLSI applications. It consists of three parts: In the first part, a contactless optical technique for mapping and determination of film and substrate carrier lifetimes in SIMOX (Separation by IMplantation of OXygen) SOI wafers has been developed for evaluating the quality of incoming wafer lots to avoid fabricating VLSI circuits on poor quality SOI materials. In the second part, two electrical characterization techniques using test structures of thick- and thin-film SOI MOSFETs for determining the interface properties of the SOI devices are presented. In the third part, analysis of current-voltage characteristics and extraction of small-signal parameters for fully depleted SOI MOSFETs are discussed.

Mapping of the film and substrate carrier lifetimes in a SIMOX wafer has been carried out by using a contactless dual beam optical modulation (DBOM) technique.

The DBOM method is based on the modulation of transmission intensity of an infrared (IR) probe-beam by a visible pump-beam (h$\nu \geq E_g$) via free carrier absorption in the SIMOX wafer. A theoretical model has been developed to extract the excess carrier lifetimes from the DBOM technique.

The modified High-Low-Frequency (HLF) transconductance method is applied to characterize the properties of film/front-gate-oxide and film/buried-oxide interfaces of partially and fully depleted SOI MOSFETs operating in linear region. A new threshold voltage method is developed for characterizing the interface state densities profile in thin (fully depleted) film SOI MOSFETs. This technique is particularly attractive since it requires only simple static drain current measurements.

The current-voltage characteristics for a fully depleted SOI MOSFET is analyzed by relating the inversion charge density to the front surface potential from the theories developed for bulk Si and SOI MOSFETs. The analysis, which is valid for back surface depletion and accumulation, gives correctly the threshold voltage, the drain current, and the transconductance in all regions of operation. The charge-sheet model and strong-inversion assumption are used in this analysis. Based on the current-voltage characteristics and charge-neutrality relation, small-signal parameters for a thin-film SOI MOSFET are extracted.

CHAPTER 1
INTRODUCTION

1.1 Silicon-on-Insulator Fabrication Technologies

The silicon-on-insulator (SOI) technology is becoming increasingly important for VLSI applications due to its advantages of simple isolation, high speed, high packing density, operating at high temperature, and radiation hardness [1-9]. In addition, the thin (fully depleted) film SOI device structure has been shown to have many advantages over the bulk silicon design, such as sharp subthreshold slope, reduced hot-electron degradation, ameliorated short-channel effects, high carrier mobility, and increased drain current [10-17]. There are a variety of techniques for fabricating the SOI structure, including SIMOX (Separation by IMplantation of OXygen), wafer bonding and etchback, Full Isolation by Porous Oxidized Silicon (FIPOS), the recrystallization of polysilicon, epitaxial lateral overgrowth (ELO), and SIMOX wafer bonding (SWB) [18-23]. The most mature among all these techniques is the SIMOX technique, while the wafer bonding technologies are potentially advantageous for the future SOI structures due to its high film quality and reproducibility. However, much effort, both on materials and devices, still needs to be made to bring SOI technology to production status.

1.1.1 SIMOX Process

As shown in Fig. 1.1 [24], a SIMOX wafer is prepared by implanting a silicon wafer with oxygen ions at a beam energy of 150 to 200 KeV and with an oxygen dose of typically 1.2 to 2.4×10^{18} cm^{-2}, followed by a high-temperature annealing at 1250 to 1350 °C [18,25]. The wafer is typically heated to 400 to 650 °C during the oxygen implantation process [2]. Precipitates and threading dislocations are dominant defects in the top silicon film after the high-temperature annealing [26]. A defect density of 10^8 to 10^9 cm^{-2} has been found for single high-dose implantation SIMOX wafers. By multiple cycles of implantation and annealed steps, dislocation density can be reduced to as low as 10^3 cm^{-2} [27]. Ultrathin uniform SOI film and good electrical characteristics have been obtained for devices and circuits built on SIMOX wafers [28]. However, the quality of buried oxide layer for a SIMOX wafer still needs to be improved. These include defects reduction in the buried oxide layer, increasing oxide breakdown voltage, and reducing film/buried-oxide interface states density.

SIMOX technology is particularly useful for applications in radiation-hardened ICs, power ICs, telecommunication ICs, submicron CMOS, and novel-devices. Fully functional units of a high speed mask configurable 256K SRAM have been fabricated on a 0.8 μm minimum geometry process built on a SIMOX substrate for harsh radiation environments [29].

1.1.2 Wafer Bonding Process

In contrast to SIMOX technology, the wafer bonding technique provides high quality and more flexibility for both SOI film and buried oxide layer. As shown in Fig. 1.2, three basic steps are required for the wafer bonding process [19]: (i) mating two wafers together at room temperature, (ii) annealing the bonded wafers at temperature above 800 °C for several hours to increase bonding strength, and (iii) thining down one of the two wafers to a proper thickness by grinding and polishing and/or etching. The major disadvantage of wafer bonding technology is difficulty in producing extremely thin uniform Si films. Therefore, the third step is becoming more important for producing ultrathin Si films with good uniformity. By using plasma etching, silicon film thicknesses less than 100 nm have been achieved with uniformity better than 10 percent [30].

The immediate application of wafer bonding technology is in CMOS and BJT circuits. It is also a potential asset for the integration of low-voltage control circuits with high-voltage circuits in power ICs. A linear power supply has been built in high-voltage bonded wafer technology [31].

1.1.3 SIMOX Wafer Bonding Process

The complementary nature of the two main technologies (SIMOX and wafer bonding) suggests the possibility of transferring the SIMOX layer on thermally oxidized Si wafers by SIMOX wafer bonding method [23]. The SWB technique retains the advantages of both SIMOX and wafer bonding technologies and eliminates their respective problems. Figure 1.3 shows the SWB process. A SIMOX wafer and an oxidized Si wafer are placed face-to-face with a gap of about 1.5 mm. After cleaning and drying the surfaces, the two wafers are brought into contact at room temperature followed by an annealing at temperatures above 960 °C. The annealed wafer pairs are then thinned in KOH solution to etch Si substrate. Finally, the buried oxide layer is removed by a buffer oxide etching (BOE) solution.

Although complicated processes are involved in SWB technology, it combines advantages of two major SOI technologies (SIMOX and wafer bonding) and can be used in the field of application for SIMOX technology.

1.2 Characteristics of SIMOX SOI Materials and Devices

Among the potential applications of SOI technologies for radiation-hardened, high-speed devices, submicron CMOS, and novel-devices [32-35], SIMOX technology is attracting the most attention because of the excellent material characteristics. Furthermore, SIMOX-based ICs address the need for military (e.g., radiation-hard SRAM) and high-voltage IC applications [36]. A typical SIMOX SOI structure consists of a Si substrate, a buried oxide with thickness of 200 to 400 nm, and a top Si superfacial layer with thickness of 100 to 300 nm above the buried oxide. Inspite of its relatively short history, the SIMOX has become the leading SOI technology. High quality Si film has been achieved in SIMOX wafers, which is essential for VLSI applications.

1.2.1 Properties of the Top Si Layer

Many diagonstic techniques, including transmission electron microscope (TEM), Rutherford backscattering spectrometry (RBS), x-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS), Raman scattering, conductivity and Hall-effect measurments, photoluminescence spectroscopy, current deep-level transient spectroscopy (C-DLTS), and photoinduced current transient spectroscopy have been applied to characterize the properties of top Si layer followed annealing at different temperatures [26,37-45]. From Raman scattering measurements, the top Si layer is under tensile strain, whose origin is due to oxide precipitates. The tensile strains were found to decrease with increasing annealing temperatures and disappear with lamp annealing at 1405 °C for half an hour. The other dominant defect is threading dislocations. The dislocation density decreases with increasing annealing temperature, but reaches a saturation value of about 10^3 cm^{-2} for multi-implanted samples annealed at $T \geq 1250$ °C [27]. For annealing at a temperature below 1300 °C, hole trap levels of 0.44 eV and 0.63 eV above the valence-band edge in the top Si layer were found by current DLTS measurements [43,44]. The conductivity and Hall-effect measurements yield a hole mobility value of about 200 $cm^2/V\cdot sec$ at room temperature, which is nearly constant in the top 100 nm of the film but drops rapidly in the interface region containing implant-induced defects for annealing at 1150 °C. When annealed at temperatures above 1300 °C, the quality of SIMOX film is greatly improved (approached to that of bulk Si), and oxygen thermal donors (TDs) are generated due to oxygen clusters distributed in the film and near the film/buried-oxide interface [38-41].

1.2.2 Properties of the Buried Oxide

Uniformity and contaminations in the buried oxide of SIMOX wafers have been studied by TEM, RBS, SIMS, and ellipsometery [26,46-48] techniques. Copper was found to be the dominant impurity while lesser amounts of iron, titanium, and chromium were also found during the formation of silicon-on-insulator structures by high fluence of oxygen implantation. The total fluence of copper introduced into the surface of a top Si layer is approximately 1 ppm of the implanted oxygen dose. Post-implantation annealing causes the copper impurity to diffuse from the surface of Si film to the buried oxide and is captured in the dislocation sites. Most of the copper impurities move to several micrometers beneath the buried oxide layer and none remain in the oxide layer [46,47]. From the ellipsometry measuements, no differences were observed in the optical properties of the thermal and synthesized (buried) oxide. The refractive index of the buried oxide is near constant (1.45) and identical to that of the thermal oxide. The measurements also reveal the presence of an intermediate layer (10 to 30 nm thick with higher and variable refractive index) at the interface between the buried oxide and the bulk silicon substrate [48].

1.2.3 Interface Characterization of SIMOX MOSCs and MOSFETs

The three main interfaces of SIMOX SOI wafers can be characterized from measurements performed on front and back faces of MOS transistors and capacitors. The properties are dependent on the technology and show a general nonuniformity along the structure. MOS capacitors in SIMOX SOI were analyzed between gate and substrate, gate and film, or substrate and film [49,50]. From high-frequency C-V measurements, the fixed oxide charge, interface traps, and doping densities are obtained for both buried oxide interfaces as well as the thickness of the buried oxide layer. From C-t (Zerbst) measurements, minority carrier generation lifetimes are calculated for the top Si film and substrate [49]. MOSFETs fabricated on SIMOX SOI wafers were shown to have good performance characteristics [10-17]. However, they also showed incompatible electrical characteristics inherent in floating bodies, including kink effect [51-53] and single-transistor latch [54]. Charge pumping and dynamic transconductance techniques have been employed for the characterization of interface states in SOI MOSFETs [55,56]. The dynamic transconductance technique is used to measure the interface-state density profile at both interfaces of the buried oxide for the full-depleted SOI MOSFETs by using the imaginary part of the measured dynamic transconductance [56]. Since a body contact is required, the charge pumping technique is not available for very thin and small SOI MOSFETs.

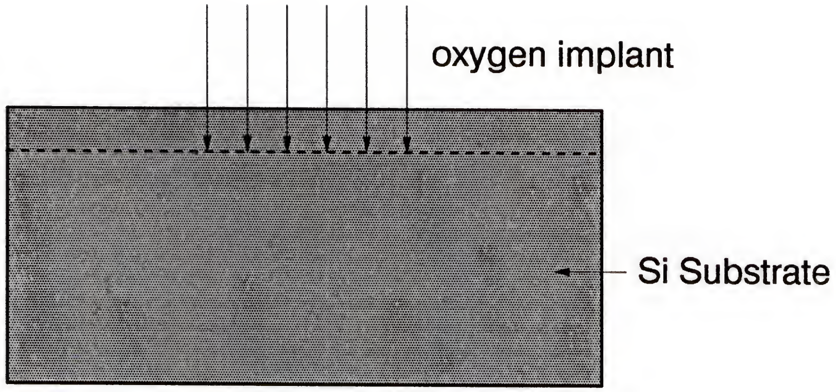
1.3 Synopsis of Chapters

This dissertation mainly deals with the development of new characterization techniques and the modeling of thin-film SOI materials and devices for VLSI applications. There are three basic objectives: (1) develop a contactless optical technique for determining and mapping of substrate and film carrier lifetimes in SIMOX SOI wafers, (2) develop electrical characterization techniques using test structures of thick- and thin-film SOI MOSFETs for measuring the interface state densities at both front-gate-oxide/Si-film and Si-film/buried-oxide interfaces, and (3) analyze current-voltage characteristics and extract small-signal parameters for fully depleted SOI MOSFETs.

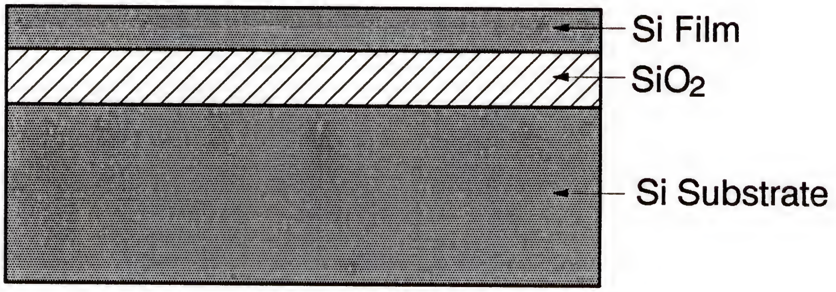
Chapter 2 describes the theoretical and experimental aspects of the substrate carrier lifetime measurements on SIMOX samples by a contactless dual beam optical modulation (DBOM) technique. A generalized model for the DBOM technique is developed. It is shown that the substrate carrier lifetimes in SOI wafers can be determined when a He-Ne CW laser (λ=6328 $\mathring{A}$) is used as the pump beam. In Chapter 3, the DBOM technique is applied for determining and mapping the film carrier lifteime profile in a SIMOX SOI wafer by using a near UV pump beam (He-Cd CW laser, λ=0.44 μm).

Chapter 4 presents a high-low-frequency (HLF) transconductance technique for extracting the interface state densities in partially and fully depleted SOI MOSFETs operating in the linear region. The modified HLF transconductance method has been successfully applied to characterize the properties of film/front-gate-oxide and film/buried-oxide interfaces of the SOI MOSFETs. A new threshold voltage method for characterizing the interface state density profile in thin (fully depleted) film SOI MOSFETs is described in Chapter 5. This technique is particularly attractive since it requires only simple static drain current measurements.

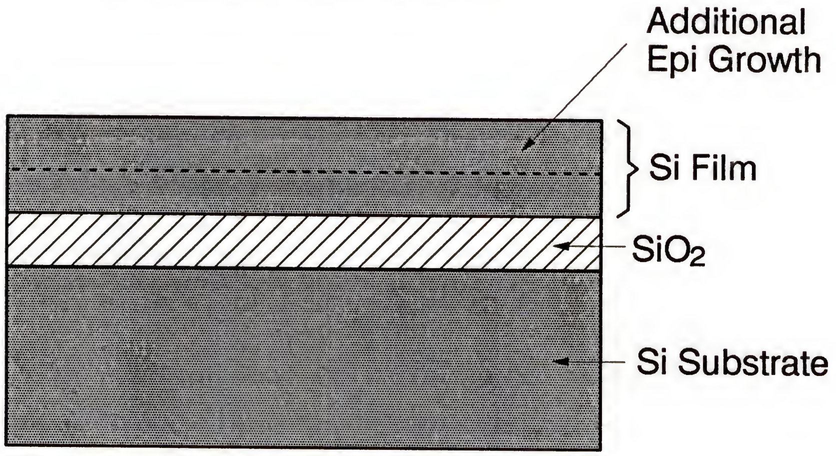
In Chapter 6, the current-voltage characteristics for the fully depleted SOI MOSFETs are analyzed. In the analysis, the inversion charge density is related to the front surface potential by the theories developed for bulk and thin-film SOI MOSFETs. The analysis, which is valid for back surface depletion and accumulation, describes correctly the threshold voltage, the drain current, and the small signal parameters in all regions of operation. The charge-sheet model and strong-inversion assumption are used in this analysis. Chapter 7 deals with the small-signal equivalent circuit for the fully depleted SOI MOSFETs by emphasizing the structural uniqueness of the devices. Under quasistatic condition, the equivalent circuit elements (e.g., intrinsic capacitances) valid for all regions of operation, including weak and moderate inversion, are derived and computed by using the theory proposed in Chapter 6. The numerical results of these parameters for both back surface depletion and accumulation are presented and compared to that of the strong-inversion assumption. Finally, key conclusions of this work are given in Chapter 8.



(a) Implant O into Si substrate.



(b) Anneal: 1250-1350 °C.



(c) Grow epi Si layer.

Figure 1.1 Separation by IMplantation of OXygen (SIMOX) process for SOI structures.

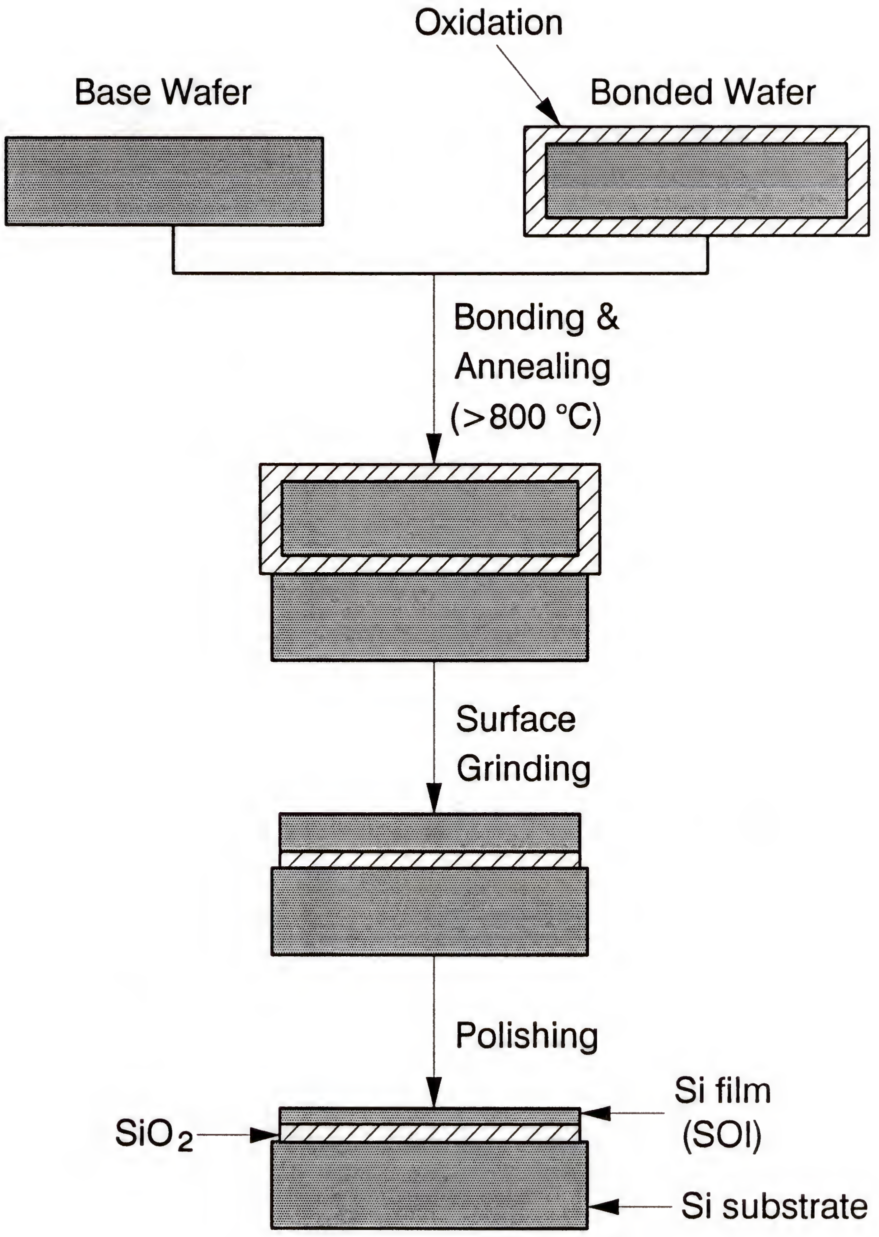


Figure 1.2 Wafer bonding process for SOI structures.

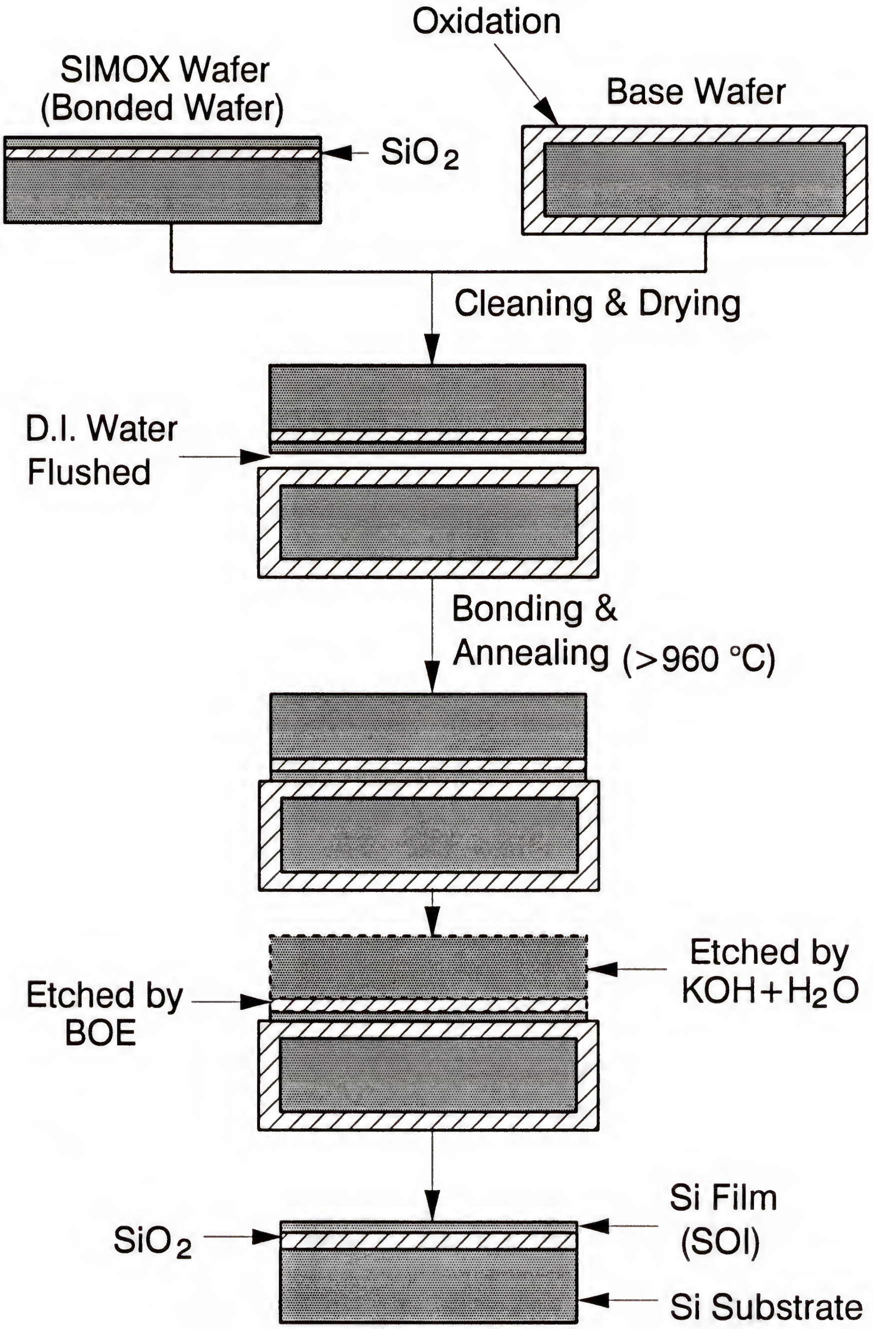


Figure 1.3 SIMOX Wafer Bonding (SWB) process for SOI structures.

CHAPTER 2
MEASUREMENTS OF SUBSTRATE CARRIER LIFETIMES IN THE SILICON-ON-INSULATOR WAFERS BY A CONTACTLESS DUAL BEAM OPTICAL MODULATION TECHNIQUE

2.1 Introduction

In integrated circuit (IC) fabrication, it is important to evaluate the quality of the starting wafers by using a quick and nondestructive technique prior to device processing. The nondestructive evaluation technique is particularly important for SIMOX (Separation by IMplantation of OXygen) circuit fabrication since there are still quality control problems for the SIMOX wafers. Although various characterization techniques [26,40,43,57] have been reported for analyzing the microstructures of buried oxide, transport properties, and bulk traps in the SOI (silicon-on-insulator) materials, it is highly desirable to develop a contactless optical technique [58-61] for determining the carrier lifetime in the SOI substrates. A SIMOX wafer is prepared by implanting a silicon wafer with oxygen ions at beam energy of 150 to 200 keV and to an oxygen dose of typically 1.2 to 2.4×10^{18} cm^{-2}, followed by a high-temperature annealing at 1250 to 1350 °C. The wafer is typically heated to 400 to 650 °C during the ion implantation process [2]. Good electrical characteristics have been obtained for devices and circuits built on SIMOX wafers [28].

In this chapter, we describe a contactless dual-beam optical modulation (DBOM) technique which has been developed for determining the substrate carrier lifetimes in the SIMOX wafers with different doping concentrations, oxygen implant doses, annealing temperatures, and film thicknesses [62]. The DBOM method is based on the modulation of the transmission intensity of an infrared (IR) probe-beam by a visible pump-beam ($h\nu \geq E_g$) via free carrier absorption in the SIMOX wafer. A theoretical model is developed to deduce the excess carrier lifetimes in the SIMOX substrate by the DBOM technique. Mappings of the substrate carrier lifetimes in these SIMOX wafers are carried out and the results are compared to values determined by the surface photovoltage (SPV) method.

2.2 Theory for the DBOM Technique

As shown in Fig. 2.1, the excess electron density in a p-type SIMOX sample as a function of distance along the x-direction can be obtained by solving the continuity equation given by

$$D_n \frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau_n} = -g_E = -\alpha \eta \phi_0 (1 - R) cos\theta_2 e^{-\alpha x} \tag{2.1}$$

where D_n is the diffusion coefficient of electrons, τ_n is the electron lifetime, g_E is the external generation rate, α is the optical absorption coefficient, η is the quantum efficiency, R is the reflectivity, and ϕ_0 is the photon flux density (*i.e.*, $\phi_0 = I_0/h\nu$, where I_0 is the incident light intensity). The boundary conditions at x=0 and x=t_f are given by

$$D_n \frac{\partial \Delta n}{\partial x}|_{x=0} = s_1 \Delta n|_{x=0} \tag{2.2}$$

and

$$-D_n \frac{\partial \Delta n}{\partial x}\Big|_{x=t_f} = s_2 \Delta n|_{x=t_f} \tag{2.3}$$

where s_1, s_2 are the surface recombination velocities at the air/Si-film and Si-film/SiO_2 interfaces, respectively, and t_f is the top Si film thickness. Using the boundary conditions given by Eqs. (2.2) and (2.3), the general solution of Eq. (2.1) for the excess electron density in the top silicon film is given by

$$\Delta n_1(x) = c_1 e^{x/L_f} + c_2 e^{-x/L_f} + c_3 e^{-\alpha x} \tag{2.4}$$

where

$$c_1 = \frac{c_3}{2}\frac{(s_1+\alpha D_n)(s_2-\frac{D_n}{L_f})e^{-t_f/L_f}-(s_1+\frac{D_n}{L_f})(s_2-\alpha D_n)e^{-\alpha t_f}}{\frac{D_n}{L_f}(s_1+s_2)cosh(\frac{t_f}{L_f})+[s_1s_2+(\frac{D_n}{L_f})^2]sinh(\frac{t_f}{L_f})}, \tag{2.5}$$

$$c_2 = -\frac{c_3}{2}\frac{(s_1+\alpha D_n)(s_2+\frac{D_n}{L_f})e^{t_f/L_f}-(s_1-\frac{D_n}{L_f})(s_2-\alpha D_n)e^{-\alpha t_f}}{\frac{D_n}{L_f}(s_1+s_2)cosh(\frac{t_f}{L_f})+[s_1s_2+(\frac{D_n}{L_f})^2]sinh(\frac{t_f}{L_f})}, \tag{2.6}$$

and

$$c_3 = -\frac{\alpha\eta\tau_f\phi_0(1-R)cos\theta_2}{\alpha^2L_f^2-1} \tag{2.7}$$

Here $L_f = (D_n\tau_f)^{1/2}$ and τ_f denote the diffusion length and lifetime of electrons in the Si film, respectively.

Similarly, the boundary conditions for the excess electron density in the p-type Si substrate are given by

$$D_n\frac{\partial\Delta n}{\partial x}\Big|_{x=t_f+t_{ox}} = s_3\Delta n|_{x=t_f+t_{ox}} \tag{2.8}$$

and

$$\Delta n|_{x\to\infty} = 0 \tag{2.9}$$

where s_3 is the surface recombination velocity at the SiO_2/substrate interface. As shown in Fig. 2.1, the generation rate g_E in the substrate can be written as

$$g_E = \alpha\eta\phi_2(1-R)cos\theta_2 e^{-\alpha[x-(t_f+t_{ox})]} \tag{2.10}$$

where ϕ_2 is the photon flux density at $x = t_f + t_{ox}$. Using Fresnel's equations, the solution for ϕ_2 is given by

$$\phi_2 = \phi_0 e^{-\alpha(t_f/cos\theta_2)}\left(\frac{2n_{si}cos\theta_2}{n_{si}cos\theta_2+n_{ox}cos\theta_3}\right)^2\left(\frac{2n_{ox}cos\theta_3}{n_{ox}cos\theta_3+n_{si}cos\theta_2}\right)^2 \tag{2.11}$$

where n_{si} and n_{ox} are the refractive index of Si and SiO_2, respectively. Now substituting Eqs. (2.10) and (2.11) into Eq. (2.1) and using the boundary conditions given by Eqs. (2.8) and (2.9), we obtain a general solution for the excess-electron density in the substrate

$$\Delta n_2(x) = c_4 e^{-[x-(t_f+t_{ox})]/L_s} + c_5 e^{-\alpha[x-(t_f+t_{ox})]}, \tag{2.12}$$

where

$$c_4 = -c_5 \frac{\alpha L_s^2 + s_3 \tau_s}{L_s + s_3 \tau_s}, \tag{2.13}$$

and

$$c_5 = -\frac{\alpha \eta \tau_s \phi_2 (1 - R) cos\theta_2}{\alpha^2 L_s^2 - 1} \tag{2.14}$$

Here $L_s = (D_n \tau_s)^{1/2}$ is the diffusion length of electrons, and τ_s is the excess electron lifetime in the subatrate.

If the excess electron and hole concentrations are equal (*i.e.*, $\Delta n = \Delta p$), then the change of optical absorption coefficient due to the short-wavelength pump beam (h$\nu \geq$E$_g$) can be written as [58-60]

$$\Delta \alpha_{\mathrm{fc}} = \sigma_{\mathrm{fc}} \Delta n \tag{2.15}$$

where $\sigma_{\mathrm{fc}}=\sigma_e+\sigma_h$ is the total optical absorption cross section of electrons and holes, and $\Delta n=\Delta n_1+\Delta n_2$ is the total excess carrier density generated in the film and the substrate. Thus, the fractional change in the transmitted beam intensity $\Delta I/I$ can be expressed by [59,61]

$$\begin{aligned} \Delta I/I &= exp\left(-\sigma_{\mathrm{fc}} \int_0^d \Delta n(x) dx\right) - 1 \\ &= exp\left[-\sigma_{\mathrm{fc}} \left(\int_0^{t_f} \Delta n_1(x) dx + \int_{t_f+t_{ox}}^d \Delta n_2(x) dx\right)\right] - 1 \end{aligned} \tag{2.16}$$

where d is the sample thickness. Solving Eqs. (2.4), (2.12), and (2.16) yields

$$ln\left(\frac{\Delta I}{I} + 1\right) = -\sigma_{\mathrm{fc}}\{L_f[c_1(e^{t_f/L_f} - 1) - c_2(e^{-t_f/L_f} - 1)] + L_s c_4 - \alpha^{-1}[c_3(e^{-\alpha t_f} - 1) - c_5]\} \tag{2.17}$$

For thin silicon film ($t_f/L_f \ll$1), Eq. (2.17) can be written as

$$\begin{aligned} \frac{\Delta I}{I} \approx\ & -\sigma_{\mathrm{fc}} \alpha \eta \phi_0 (1 - R) cos\theta_2 \left[\left(L_s \frac{\alpha L_s^2 + s_3 \tau_s}{L_s + s_3 \tau_s} - \frac{1}{\alpha}\right)\left(\frac{\phi_2/\phi_0}{\alpha^2 L_s^2 - 1}\right) \tau_s \right. \\ & \left. + \left(\frac{[\alpha^2 D_n^2 - (D_n/L_f)^2]}{D_n(s_1 + s_2) + t_f[s_1 s_2 + (D_n/L_f)^2]}\right)\left(\frac{\alpha^{-1} t_f (1 - e^{-\alpha t_f})}{\alpha^2 L_f^2 - 1}\right) \tau_f \right] \end{aligned} \tag{2.18}$$

In Eq. (2.18) we have approximated $ln[(\Delta I/I) + 1] \approx \Delta I/I$ for $\Delta I/I \ll$1. Equation (2.18) can be further simplified by assuming that (i) $\alpha^2 L_s^2$, $\alpha^2 L_f^2 \gg$1, which is true for $\alpha > 1\times 10^3$ cm^{-1}, (ii) $L_s \gg s_3\tau_s$ for small interface recombination velocity at the SiO$_2$/substrate interface, and (iii) $D_n \gg s_1 s_2 \tau_f$. Since a typical surface recombination velocity s_1 at air/Si-film interface is about 10^2 cm/s [63], $D_n \approx 33.7$ cm^2/s at 300 K [64], and s_2 at Si-film/SiO$_2$ interface is about 1-10 cm/s [63], assumption (iii) is valid for $\tau_f < 10^{-2}$ sec. In general, upon irradiation, s_1 was found to increase with its peak value at about 10^6 cm/sec [65]. Thus, assumption (iii) is still true for $\tau_f < 10^{-6}$ s, and Eq. (2.18) can be simplified to

$$\frac{\Delta I}{I} \approx -\sigma_{\mathrm{fc}}\eta\phi_0(1-R)cos\theta_2\tau_{eff}, \tag{2.19}$$

where

$$\tau_{eff} = \left(\frac{1-e^{-\alpha t_f}}{1+\tau_f(s_1+s_2)/t_f}\right)\tau_f + (\phi_2/\phi_0)\tau_s \tag{2.20}$$

Based on the above assumptions, the first term on the right hand side of Eq. (2.20) can be neglected, and from Eqs. (2.11) and (2.20) we obtain

$$\frac{\tau_{eff}}{\tau_s} \approx \frac{\phi_2}{\phi_0} \propto (1-\alpha t_f/cos\theta_2) \tag{2.21}$$

Note that Eq. (2.21) is obtained by using $e^{-\alpha(t_f/cos\theta_2)} \approx (1-\alpha t_f/\cos\theta_2)$ in Eq. (2.11) for $\alpha t_f/\cos\theta_2 \ll 1$. Thus, from Eq. (2.21) we can determine the carrier lifetime τ_s from the measured τ_{eff} in the SIMOX substrates by using DBOM technique.

It is noted that the above analysis can be applied equally well for holes in the n-type substrates provided that the parameters for electrons are replaced by holes (e.g., replacing D_n by D_p, and τ_n by τ_p, etc.).

2.3 DBOM Experimental Details

Figure 2.2 shows the schematic diagram of the experimental setup for the DBOM technique. The probe beam is from a tungsten lamp passing through an IR filter, with a focused beam size of about 4 mm in diameter. The IR filter is a low-doped silicon wafer, which has a cutoff wavelength of about 1.1 μm. A 1.5 mW He-Ne CW laser (λ=6328 $\AA$) is used as the pump beam, which is focused to a beam size of about 2 mm in diameter and is aligned with the probe beam. This would eliminate the 3-dimensional effect due to the spatial distribution of nonequilibrium electrons and holes [60]. Both the probe and pump beams are chopped (not simultaneously) at 400 Hz for synchronous detection by using a lock-in amplifier. A simple initial-clean process was performed on the SIMOX wafer prior to the DBOM measurement.

In the experiment, the IR transmission intensity I was first measured by turning on the chopper and tungsten light when the laser was off, and then the resulting signals were measured by a lock-in amplifier. The pump beam signal was then measured by turning on the He-Ne laser and moving the chopper away from the tungsten light to chop the laser beam when the IR probe beam was on. The measured pump beam signal was ΔI. The reflected power of the pump beam was detected by a optical power meter to determine the reflectivity R at the SOI wafer surface. To minimize the effects of stray light from the laser pump beam, optical baffles were used around the SOI wafer.

2.4 Results and Discussion

Excess carrier lifetime measurements were performed on both the n- and p-type SIMOX wafers with different epilayer thicknesses, annealing temperatures, and oxygen implant doses. From Eqs. (2.19) and (2.21), the excess carrier lifetimes in the SIMOX substrate were calculated from the measured ΔI, I, R, and using the values of $\sigma_{\mathrm{fc}} \approx 9.5\times10^{-18}$ cm^{-2} [64,66], $\alpha \approx 3.3\times10^{3}$ cm^{-1} [64], $\eta \approx 0.85$ [64], $\phi_0 \approx 1.1\times10^{17}$ cm^{-2}·sec^{-1}, θ_1=56.3° and ϕ_2 from Fig. 2.3.

The results for several SIMOX wafers are summarized in Table 2.1. In order to assess the carrier lifetime values determined by the DBOM technique, the SPV measurements were also made on two SIMOX samples to deduce the carrier lifetimes in the substrate. The results are also listed in Table 2.1. Reasonable agreement was obtained between these two methods. To verify that the measured signal is indeed due to the IR modulation beam by the free carriers generated by the pump beam, we measured the modulation light intensity ΔI as a function of IR transmission intensity I, and the result is plotted in Fig. 2.4, which shows a linear relation between ΔI and I as predicted by Eq. (2.19).

If the interface recombination velocity at the SiO_2/substrate interface is not small (*i.e.*, $L_s \gg s_3\tau_s$ is no longer held), then from Eqs. (2.18) and (2.19) by ignoring the second term in Eq. (2.18), we obtain

$$\tau_{eff} \approx \alpha L_s \left(\frac{\alpha L_s^2 + s_3\tau_s}{L_s + s_3\tau_s}\right)\left(\frac{\phi_2/\phi_0}{\alpha^2 L_s^2}\right)\tau_s \tag{2.22}$$

From Eq. (2.22), τ_s can be determined by generating different sets of (s_3, τ_s) that fit to a given effective lifetime (τ_{eff}) response, as shown in Fig. 2.5. It should be noted that Eq. (2.21) holds for $s_3 \leq 10^3$ cm/sec. In fact, on a thermally grown silicon oxide, the surface recombination velocity is in the range of 1 to 10 cm/sec [64]. Therefore, Eq. (2.21) is valid for determining τ_s in the SIMOX substrates. For $s_3 > 10^2$ cm/sec, the excess electron lifetime begins to show deviation from the excess hole lifetime. This is due to the difference in the diffusion coefficients which are 33.7 cm^2/s for electrons and 12.4 cm^2/s for holes at 300 K for the present case [64].

Figure 2.6 through Fig. 2.11 show the mappings and histograms of the substrate carrier lifetimes for different SIMOX wafers, respectively. We divided the 5-inch SIMOX wafer into 88 squares in the DBOM measurements. Thus, the area of each square shown in Figs. 2.6, 2.8, and 2.10 is about 1 cm^2. It is noted that values of carrier lifetimes in different regions of the SIMOX wafer are represented by different patterns of the squares. For example, in Fig. 2.10, pattern P_1 represents the values of τ_s varying from (17.5+17.5×15%)=20.1 to (17.5+17.5×25%)=21.9 μs (where 17.5 μs is the average τ_s), pattern P_2 is for τ_s to vary from 18.4 to 20.1 μs, and pattern P_3 is for τ_s varying from 16.6 to 18.4 μs, etc.. The patterns shown in Fig. 2.11 have the same range of carrier lifetimes as that shown in Fig. 2.10 and the height of each pattern represents the percentage of the area covered by that pattern. From Fig. 2.6 through Fig. 2.11, it is clearly shown that the uniformity and values of the excess carrier lifetimes in the SIMOX substrate will increase as the thickness of the top silicon film increases and is more uniform in the central region than near the edge of the substrate. A similar carrier lifetime profile across the SIMOX wafer was also observed in the SPV measurements for sample A4 and A5.

The theory developed here is used for extracting the excess carrier lifetimes in the SIMOX substrate. In order to determine the carrier lifetime in the top Si film, the first term of Eq. (2.20) must be comparable with the second term. In other words, the carrier lifetimes in the top Si film can not be determined by the DBOM technique if the Si film thickness or the absorption coefficient for the pump beam is too small. For example, a SIMOX wafer with $s_1 \approx 10^2$ cm/s [63], $s_2 \approx$1-10 cm/s [63], and L_f of a few micrometers, value of the first term in Eq. (2.20) is at least one order of magnitude smaller than that of the second term if the top Si film thickness is 2 μm or less. However, if the thickness of Si film is greater than 2 μm, then the first term is comparable with the second term and the carrier lifetime in the top Si film can be extracted from Eq. (2.20) by changing the incident angle θ_1 (and hence θ_2) of the pump beam. Furthermore, by using a pump-beam of shorter wavelength, the value of the first term in Eq. (2.20) will become much larger than that of the second term due to the larger absorption coefficient. Therefore, the second term in Eq. (2.20) can be neglected, and the carrier lifetime in the top Si film can be determined by using the DBOM technique.

2.5 Conclusion

In conclusion, we have demonstrated a contactless DBOM technique for determining the excess carrier lifetimes in SIMOX substrates. The technique consists of modulating the absorption of IR probe-beam passing through the wafer by excess free carriers. The excess free carriers are generated by a visible pump-beam. This method is particularly useful for monitoring the contamination and mapping the substrate carrier lifetimes of the starting SIMOX wafers. Extension of this technique for determining the carrier lifetimes in the top Si film of SOI wafers will be discussed in Chapter 3.

Table 2.1 SIMOX parameters and substrate lifetimes measured by using the DBOM and SPV methods. The five samples were implanted with oxygen dose 1.8×10^{18} cm^{-2} and annealed at 1310 °C, 5 hours for samples A1, A2 and 1285 °C, 6 hours for samples A3-A5.

Sample	Epilayer Thickness t_f (μm)	Buried Oxide Thickness t_{ox} (μm)	Substrate Resistivity (type, Ω-cm)	Averaged DBOM τ_s (μs)	Averaged SPV τ_s (μs)
A1*	0.1873	0.3791	p, 15-25	7.4	x
A2	0.2265	0.3548	n, 10-20	5.2	x
A3	0.53	0.39	n, 6	13.8	x
A4	0.85	0.39	n, 6	14.9	15.96
A5	1.65	0.39	n, 6	17.5	19.49

$*$ A1 is a multiple implant wafer with doses of 0.5, 0.5, 0.8×10^{18} cm^{-2}.

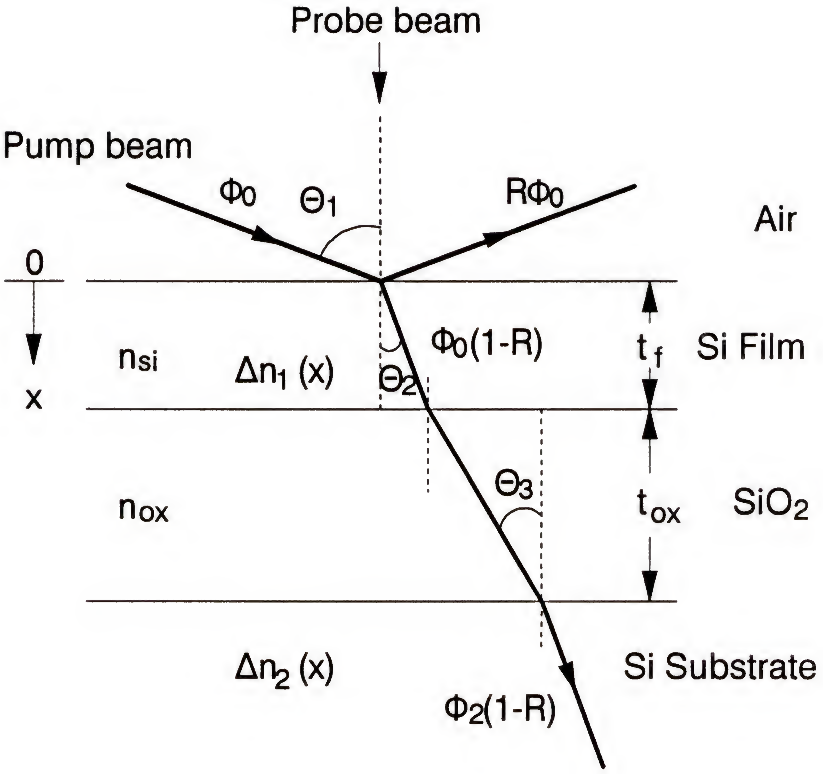


Figure 2.1 Sketch of the incident pump beam impinging on an SOI structure, which is used in the calculation of ϕ_2/ϕ_0, Δn_1(x), and Δn_2(x).

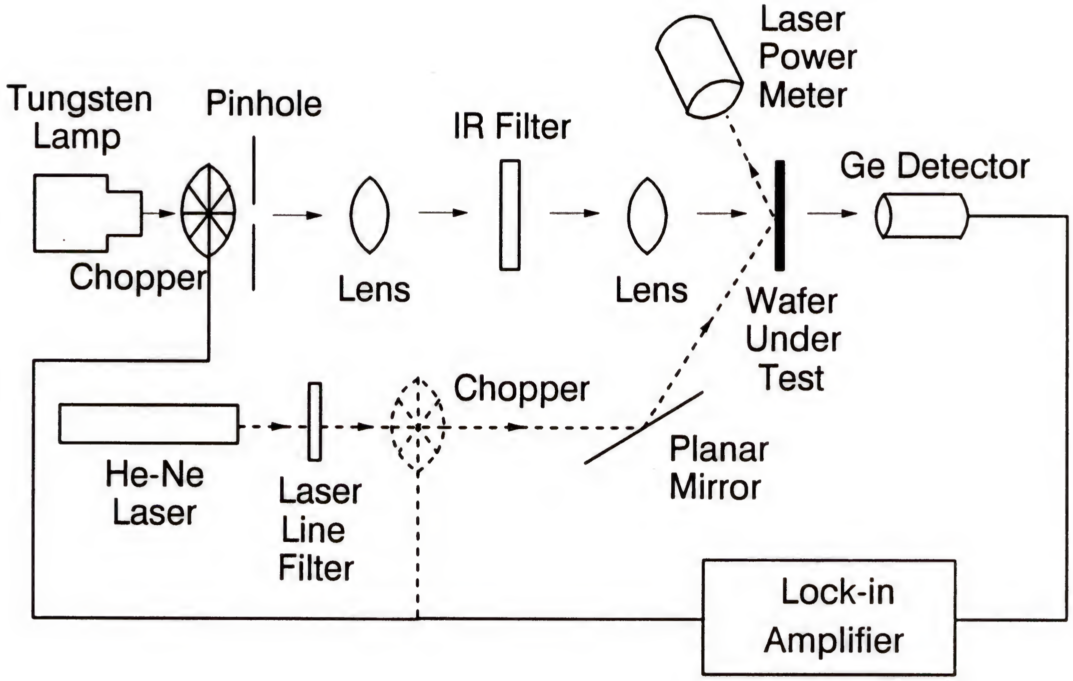


Figure 2.2 Schematic diagram for the dual beam optical modulation (DBOM) experimental setup.

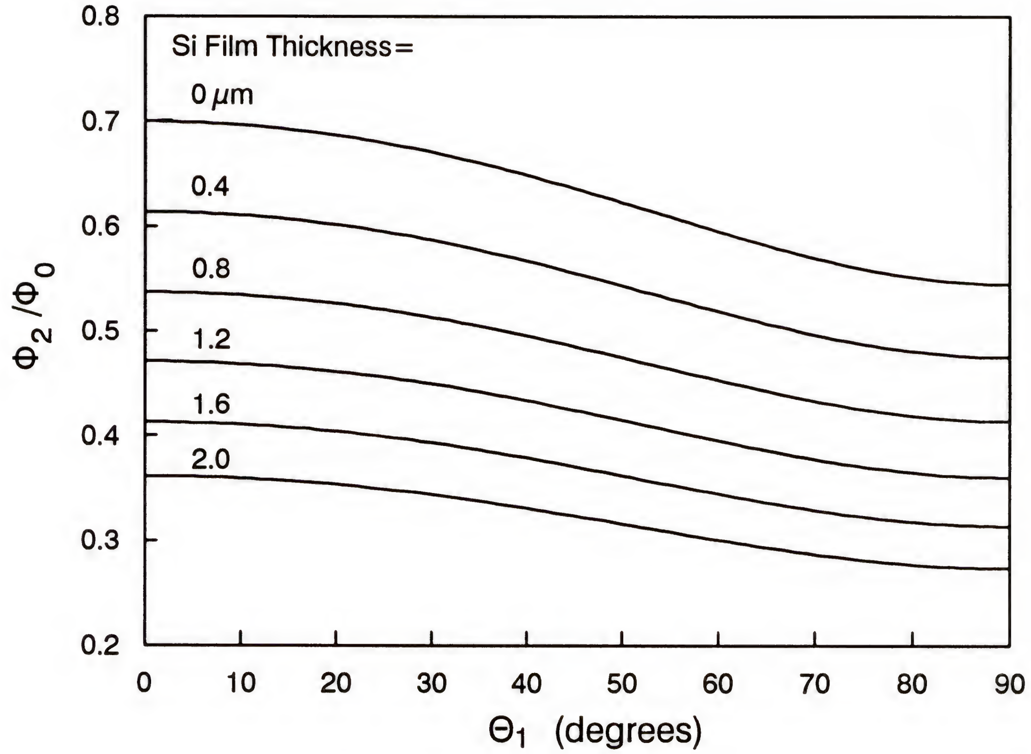


Figure 2.3 Ratio of ϕ_2/ϕ_0 calculated from Eq. (2.11) for different incident angles and Si film thicknesses.

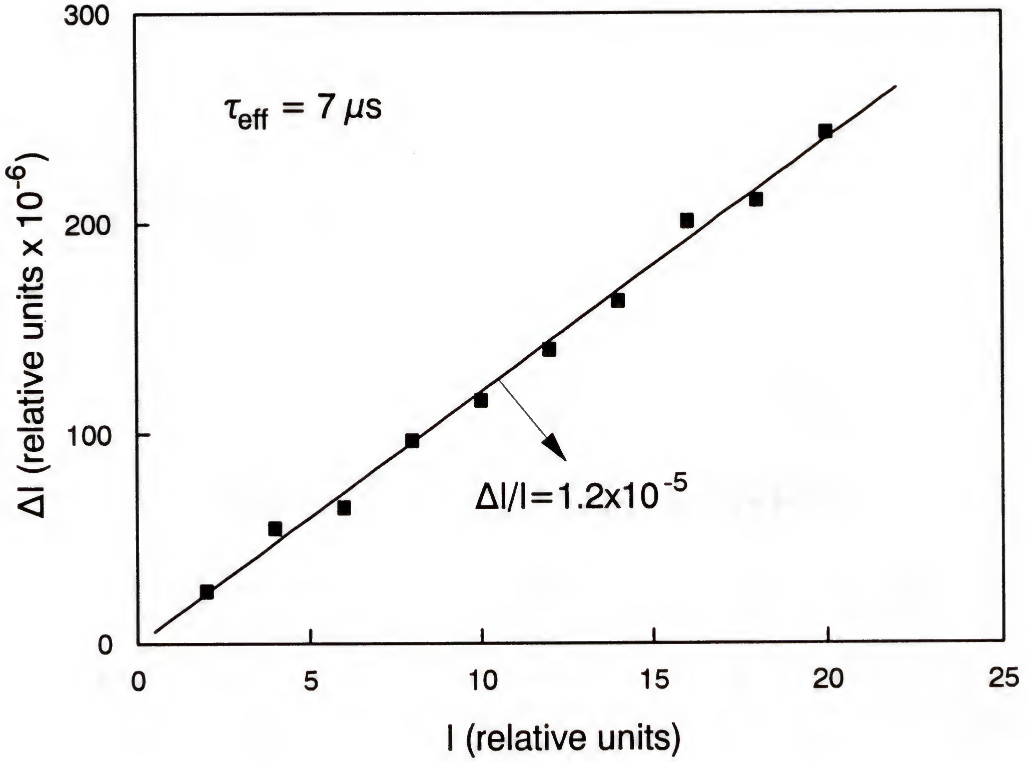


Figure 2.4 A plot of the modulation intensity ΔI as a function of the transmission intensity I of the IR probe-beam for sample A3, showing the expected linear relation.

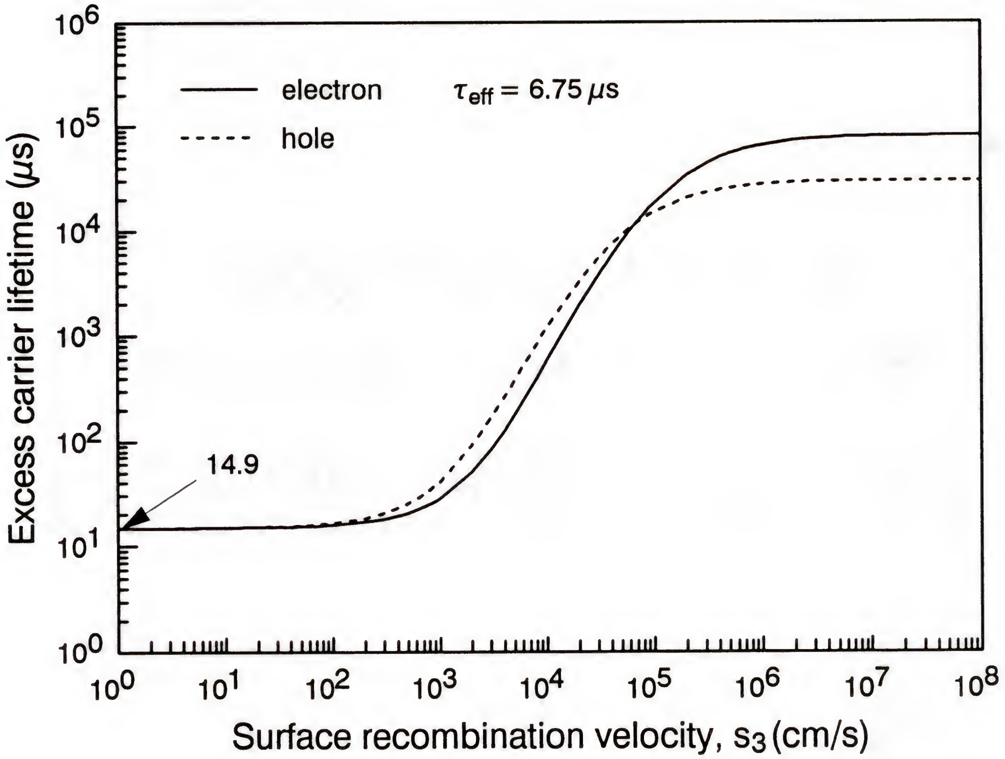


Figure 2.5 Excess carrier (electron and hole) lifetimes of the substrate (τ_s) versus interface recombination velocity at SiO_2/substrate interface (s_3) for sample A4. This is plotted for a wide range of s_3 and τ_s that fit Eq. (2.22) for a given effective lifetime (τ_{eff}) response.

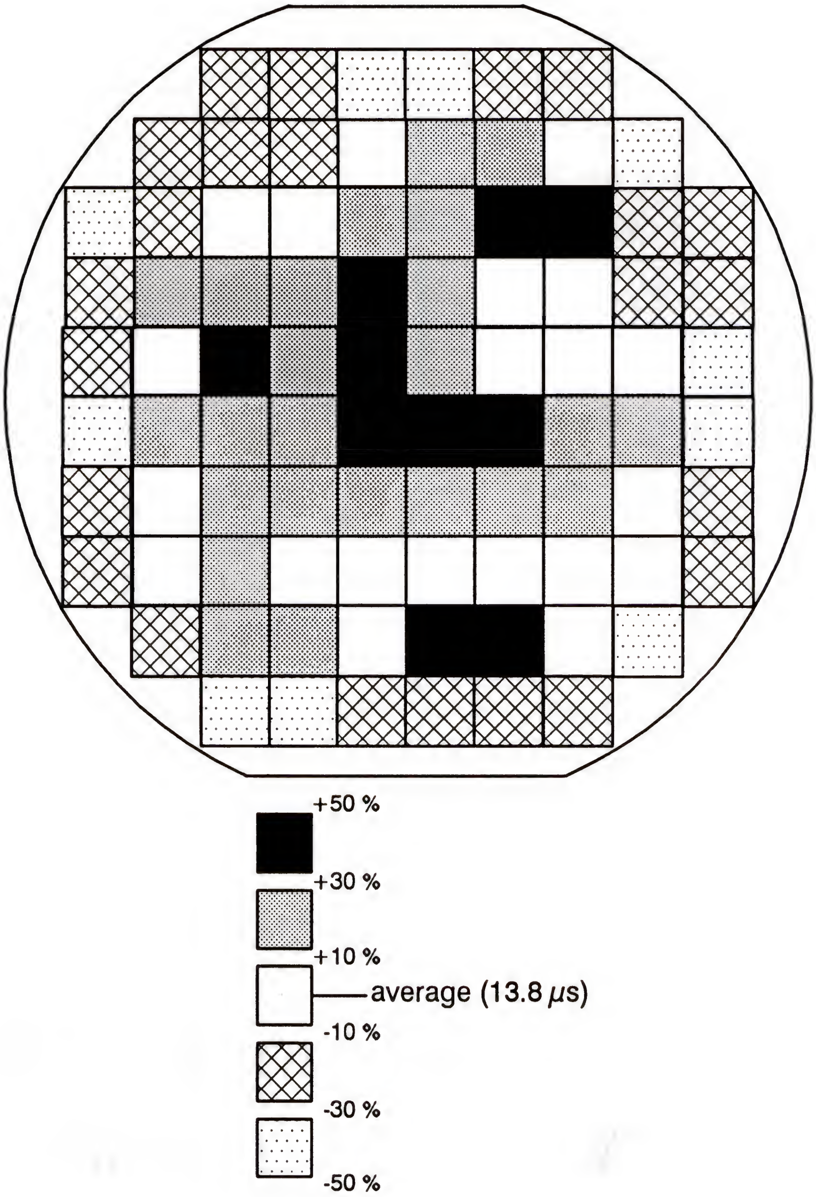


Figure 2.6 Mapping of τ_s in the SIMOX substrate for sample A3. The range of τ_s varies from 6.9 to 20.7 μs and the average value is 13.8 μs.

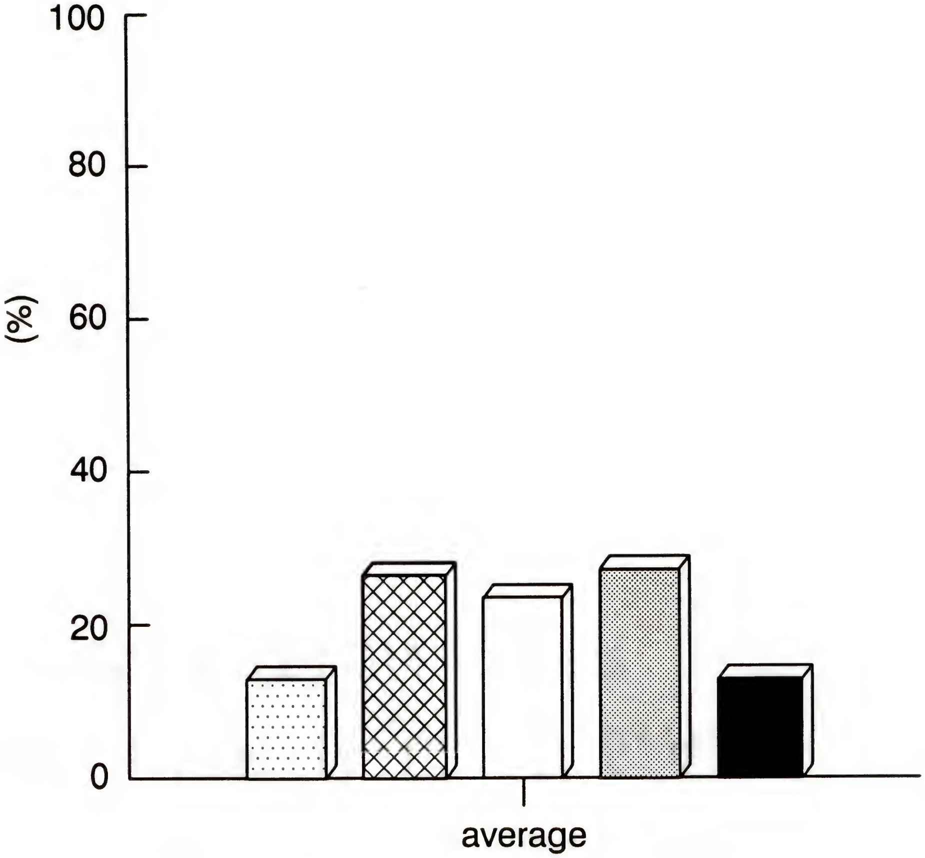


Fig 2.7 Histogram of τ_s for sample A3. The range of τ_s and the meaning of the patterns are similar to that of Fig. 2.6.

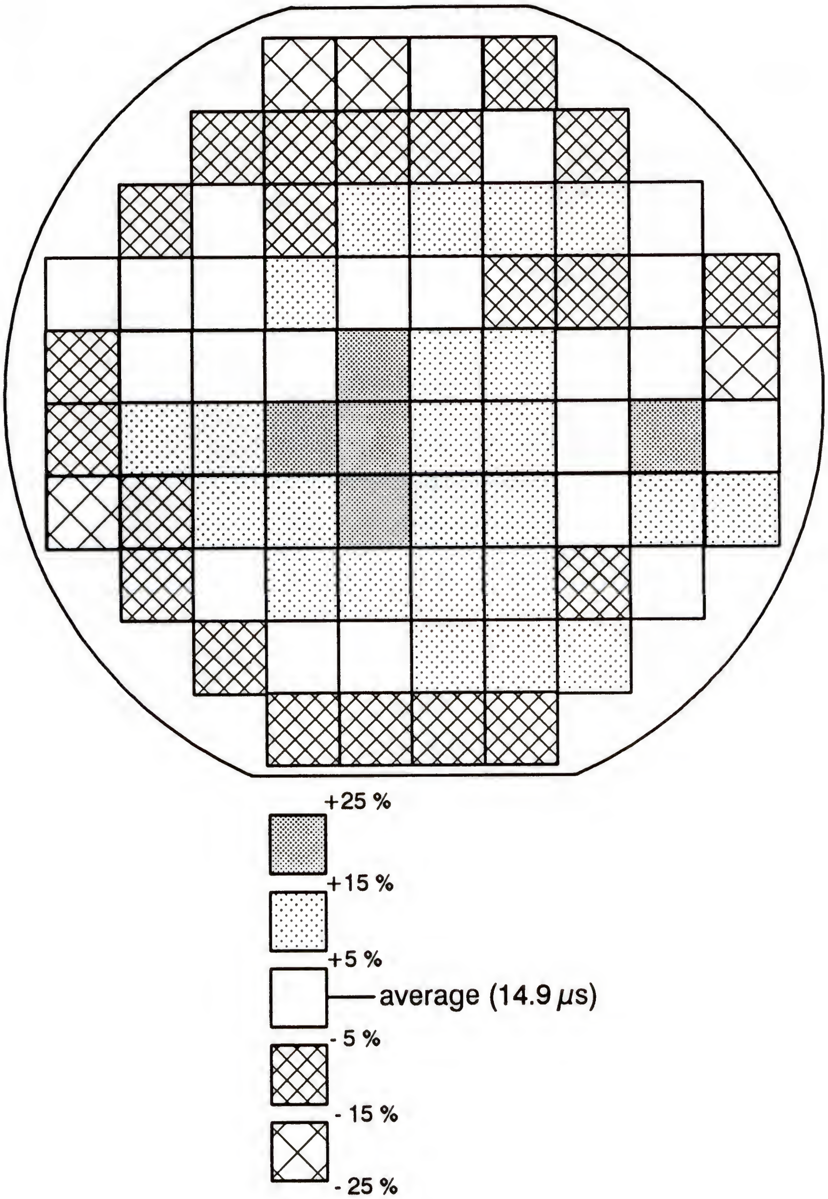


Figure 2.8 Mapping of τ_s for sample A4. The range of τ_s varies from 11.2 to 18.6 μs and the average value is 14.9 μs.

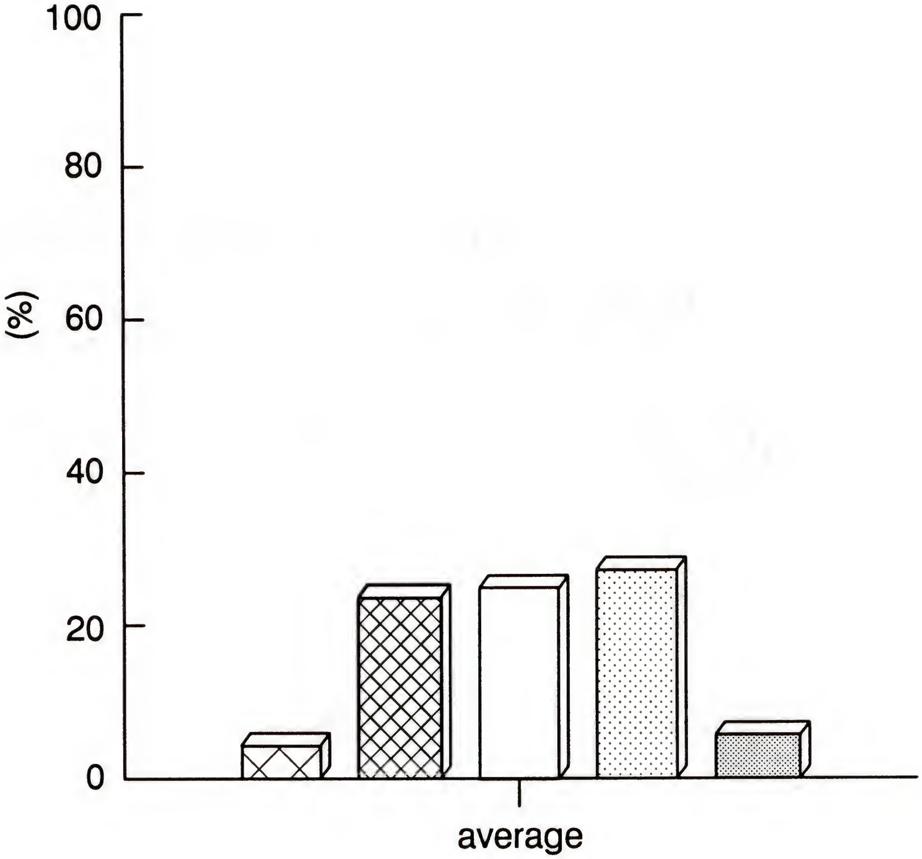


Figure 2.9 Histogram of τ_s for sample A4. The range of τ_s and the meaning of the patterns are similar to that of Fig. 2.8.

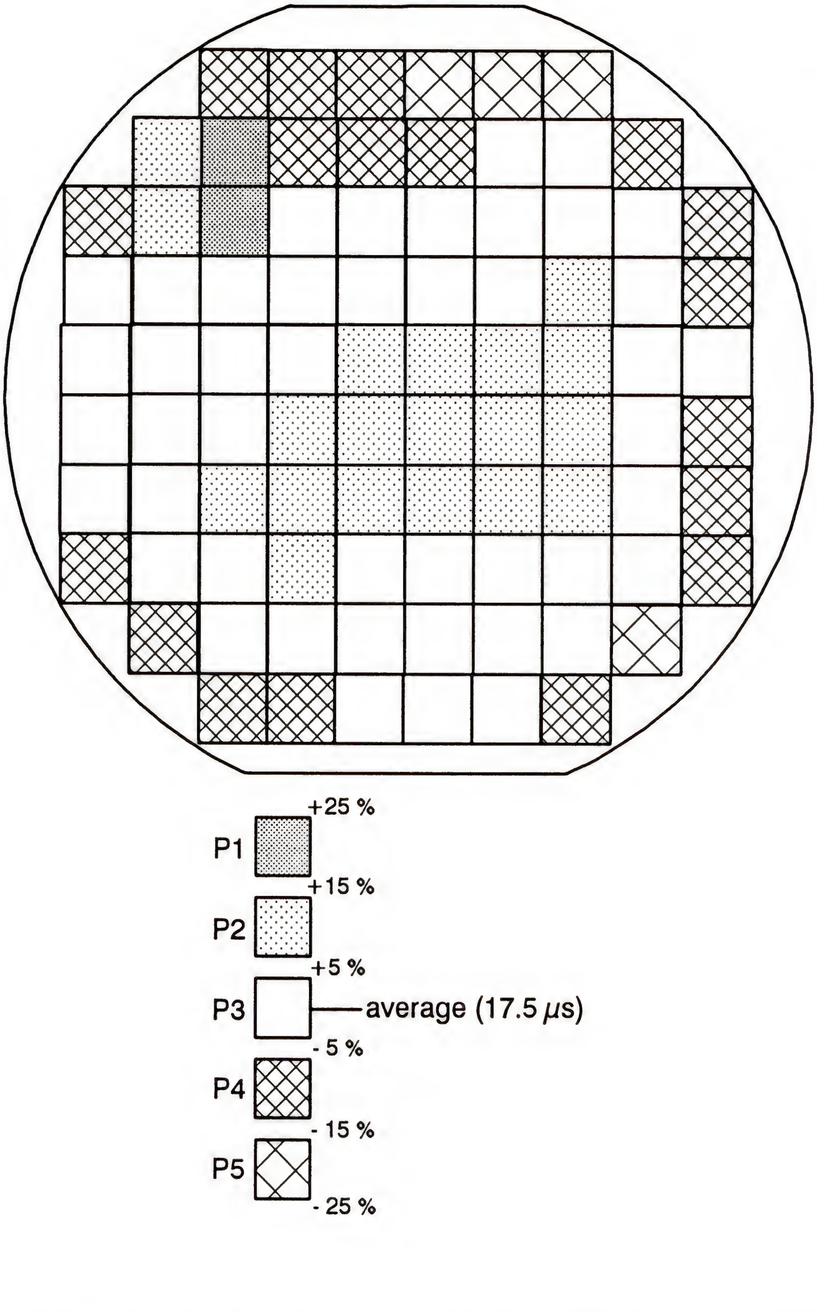


Figure 2.10 Mapping of τ_s for sample A5. The range of τ_s varies from 13.1 to 21.9 μs and the average value is 17.5 μs.

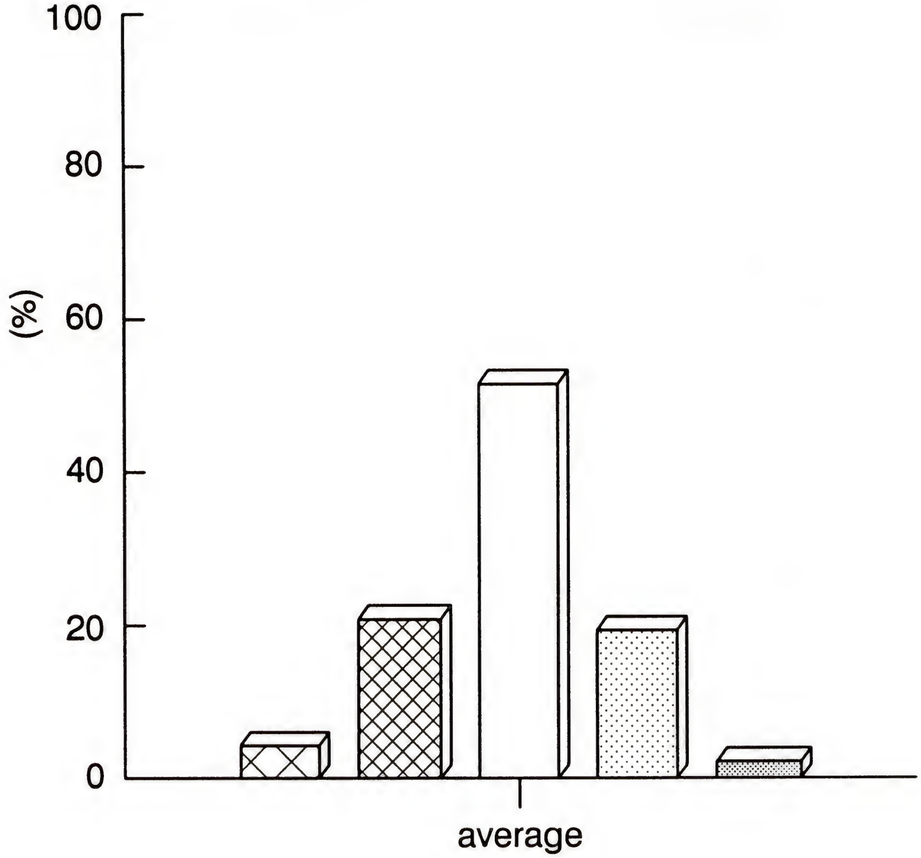


Figure 2.11 Histogram of τ_s for sample A5. The range of τ_s and the meaning of the patterns are similar to that of Fig. 2.10.

CHAPTER 3
MEASUREMENTS OF FILM CARRIER LIFETIMES IN THE SILICON-ON-INSULATOR WAFERS BY A CONTACTLESS DBOM TECHNIQUE

3.1 Introduction

The surface photovoltage (SPV) technique [66] has been widely used in minority carrier diffusion length and lifetime measurements in bulk semiconductors and SOI substrates. However, this technique is not suitable for determining the film carrier lifetime in a thin-film SIMOX wafer. This is due to the fact that the top Si film thickness t_f must be thicker than the minority carrier diffusion length for the SPV method to work. This condition can not be met in thin-film SIMOX wafers. In addition, the light source used in the SPV is usually in the wavelength range from 0.8 to 1.0 μm which is deeply penetrating into the SIMOX wafer, and thus cannot be used to determine the thin film lifetimes in the SOI materials. In Chapter 2, a DBOM technique was introduced for characterizing substrate carrier lifetimes in SIMOX wafers. In this chapter, the DBOM technique is applied to determine the film carrier lifetimes in the SIMOX wafers [67].

3.2 Extraction of Excess Carrier Lifetimes

As shown in Fig. 3.1, the fractional change in the transmitted beam intensity $\Delta I/I$ given in Eq. (2.19) can be rewritten as

$$\frac{\Delta I}{I} \approx -\sigma_{\mathrm{fc}}\eta\phi_0(1-R)cos\theta_2\tau_{eff}, \tag{3.1}$$

where

$$\tau_{eff} \approx (1-e^{-\alpha t_f})\tau_f + (\phi_2/\phi_0)\tau_s, \tag{3.2}$$

and σ_{fc} is the total absorption cross section of the excess electrons and holes, η is the quantum efficiency, ϕ_0 is the incident photon flux density, R is the reflectivity, α is the optical absorption coefficient, t_f is the thickness of Si film, τ_f is the excess carrier lifetime in the Si film, τ_s is the excess carrier lifetime in the Si substrate, and ϕ_2 is given by Eq. (2.11) as

$$\phi_2 = \phi_0 e^{-\alpha(t_f/cos\theta_2)} \left(\frac{2n_{si}cos\theta_2}{n_{si}cos\theta_2 + n_{ox}cos\theta_3}\right)^2 \left(\frac{2n_{ox}cos\theta_3}{n_{ox}cos\theta_3 + n_{si}cos\theta_2}\right)^2 \tag{3.3}$$

The first term on the right hand side of Eq. (3.2) is independent of the incident angle of the pump beam. From Eq. (3.2), τ_f and τ_s can be determined by using two incident angles θ_1 and θ_1', and the results yield

$$\tau_f = \frac{1}{1 - e^{-\alpha t_f}} \frac{\tau_{eff}\phi_2' - \tau_{eff}'\phi_2}{\phi_2' - \phi_2} \tag{3.4}$$

and

$$\tau_s = \frac{(\tau_{eff}' - \tau_{eff})\phi_0}{\phi_2' - \phi_2} \tag{3.5}$$

where τ_{eff} and τ_{eff}' are the measured effective lifetimes, and ϕ_2 and ϕ_2' are the calculated photon flux densities in the substrate region for incident angles θ_1 and θ_1', respectively. Thus, from Eq. (3.4), the film carrier lifetimes (τ_f) in the SIMOX wafers can be determined by measuring τ_{eff} as a function of the incident angle of the pump beam.

3.3 Experimental Details

The schematic diagram of the experimental setup for the DBOM technique is shown in Fig. 2.2 except that a He-Cd laser and a bandpass filter are used to replace the He-Ne laser and line filter, respectively. The probe beam is from a tungsten lamp passing through an IR filter, with a focused beam size of about 4 mm in diameter. The IR filter is a low-doped silicon wafer, which has a cutoff wavelength of about 1.1 μm. A 15 mW He-Cd CW laser (λ=4400 $\mathring{A}$) is used as the pump beam, which is focused to a beam size of about 2 mm in diameter, and is aligned with the probe beam. This would eliminate the 3-dimensional effect due to the spatial distribution of nonequilibrium electrons and holes [60]. Both the probe and pump beams are chopped at 400 Hz for synchronous detection by using a lock-in amplifier.

In the experiment, the IR transmission intensity I was first measured by turning on the chopper and tungsten light when the laser was off, and then measured the resulting signals by a lock-in amplifier. The pump beam signal was then measured by turning on the He-Cd laser and by moving the chopper away from the tungsten light to chop the laser beam when the IR probe beam was on. The measured pump beam signals were ΔI for incident angle θ_1 and $\Delta I'$ for θ_1'. The reflected power of the pump beam was detected by an optical power meter to determine the reflectivity R at angle θ_1 and R' at θ_1' on the SIMOX wafer surface. To minimize the effect of stray light from the laser pump beam, optical baffles were used around the test wafer.

3.4 Results and Discussion

Excess carrier lifetime measurements were made on both the n- and p-type SIMOX wafers with different epilayer thicknesses, annealing temperatures, and oxygen implant doses. From Eqs. (3.1), (3.4) and (3.5), the film and substrate carrier lifetimes in the SIMOX samples were calculated from the measured ΔI, $\Delta I'$, I, R, R' and using values of $\sigma_{fc} \approx 9.5\times10^{-18}$ cm^{-2} [64,66], $\alpha \approx 3\times10^{4}$ cm^{-1} [64], $\eta \approx 0.5$ [64], $\phi_0 \approx 2.5\times10^{18}$ cm$^{-2}\cdot$sec^{-1}, $\theta_1=31.8°$, $\theta_1'=62.4°$ and ϕ_2 from Fig. 3.2.

The results for several SIMOX wafers are summarized in Table 3.1, which shows that the film carrier lifetimes are one to two orders of magnitude smaller than that of the substrate carrier lifetimes. This may be attributed to the precipitates and threading dislocations which are created in the top Si film followed high-temperature annealing after oxygen implantation [26,68,69]. In order to assess the carrier lifetime values determined by the DBOM technique, the SPV measurements were also made on two SIMOX samples to deduce the carrier lifetimes in the substrate. The results are also lised in Table 3.1. Reasonable agreement was obtained between these two methods.

Figures 3.3 and 3.4 show the mapping of film carrier lifetimes for a typical SIMOX wafer. We divided the 5-inch SIMOX wafer into 88 squares for the DBOM measurements. Thus, the area of each square shown in Figs. 3.3 and 3.4 is about 1 cm^2. Values of carrier lifetimes in different regions of the SIMOX wafer are represented by different patterns of the squares. For example, in Fig. 3.3, pattern P_1 represents values of τ_f varying from $(0.23+0.23\times24\%)=0.29$ to $(0.23+0.23\times40\%)=0.32$ μs with an average τ_f of 0.23 μs, pattern P_2 is for τ_f to vary from 0.25 to 0.29 μs, and pattern P_3 is for τ_f varying from 0.21 to 0.25 μs, etc.. From Figs. 3.3 and 3.4, it is clearly shown that the uniformity of the excess carrier lifetimes in the SIMOX film will increase as the thickness of the silicon film increases, and is more uniform in the central region than near the edge of the wafer. A similar substrate carrier lifetime profile across the SIMOX wafer was also observed for samples A2, A3, A4 and A5 described in Chapter 2. The dependence of the film carrier lifetime on the film thickness is shown in Fig. 3.5 for the samples given in Table 3.1. The film carrier lifetimes increase slightly as the film thickness increases and seem to reach saturation values which depend on the parameters of processing. This can be explained by the better quality in the top layer (increases with the film thickness) of the film [38-41].

3.5 Conclusion

In this chapter, we have applied the contactless DBOM technique to determine the excess carrier lifetimes in both the film and substrate of SIMOX wafers by using a He-Cd CW laser with wavelength of 4400 $\AA$ as the pump-beam. The results showed that film excess carrier lifetimes were one to two orders of magnitude smaller than the substrate lifetimes in the SIMOX wafers. The uniformity and magnitude of the excess carrier lifetimes in the SIMOX film were found to increase as the film thickness increases. This method is particularly useful for monitoring the contamination and mapping the film carrier lifetimes in the starting SOI (especially SIMOX) wafers.

Table 3.1 The measured film and substrate excess carrier lifetimes in five SIMOX wafers with oxygen implant dose 1.8×10^{18} cm^{-2}. The anneal done at 1310 °C, 5 hours for samples A1 and A2 and 1285 °C, 6 hours for samples A3-A5.

Sample	Epilayer Thickness t_f (μm)	Buried Oxide Thickness t_{ox} (μm)	Substrate Resistivity (type, Ω-cm)	Averaged DBOM τ_f (μs)	Averaged DBOM τ_s (μs)
A1*	0.1873	0.3791	p, 15-25	0.23	7.5
A2	0.2265	0.3548	n, 10-20	0.18	5.4
A3	0.53	0.39	n, 6	0.46	14.1
A4	0.85	0.39	n, 6	0.58	15.2
A5	1.65	0.39	n, 6	0.72	17.9

$*$ A1 is a multiple-implant Si wafer with doses of 0.5, 0.5, 0.8×10^{18} cm^{-2}.

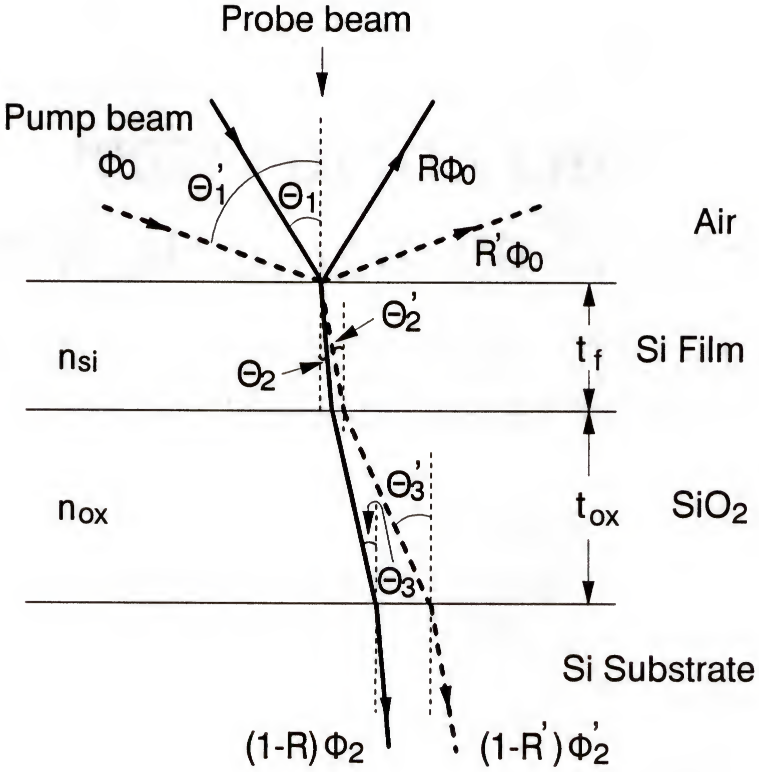


Figure 3.1 Sketch of the incident pump beam impinging on an SOI structure, which is used in the calculation of ϕ_2/ϕ_0 and the excess carrier densities generated in the film and the substrate.

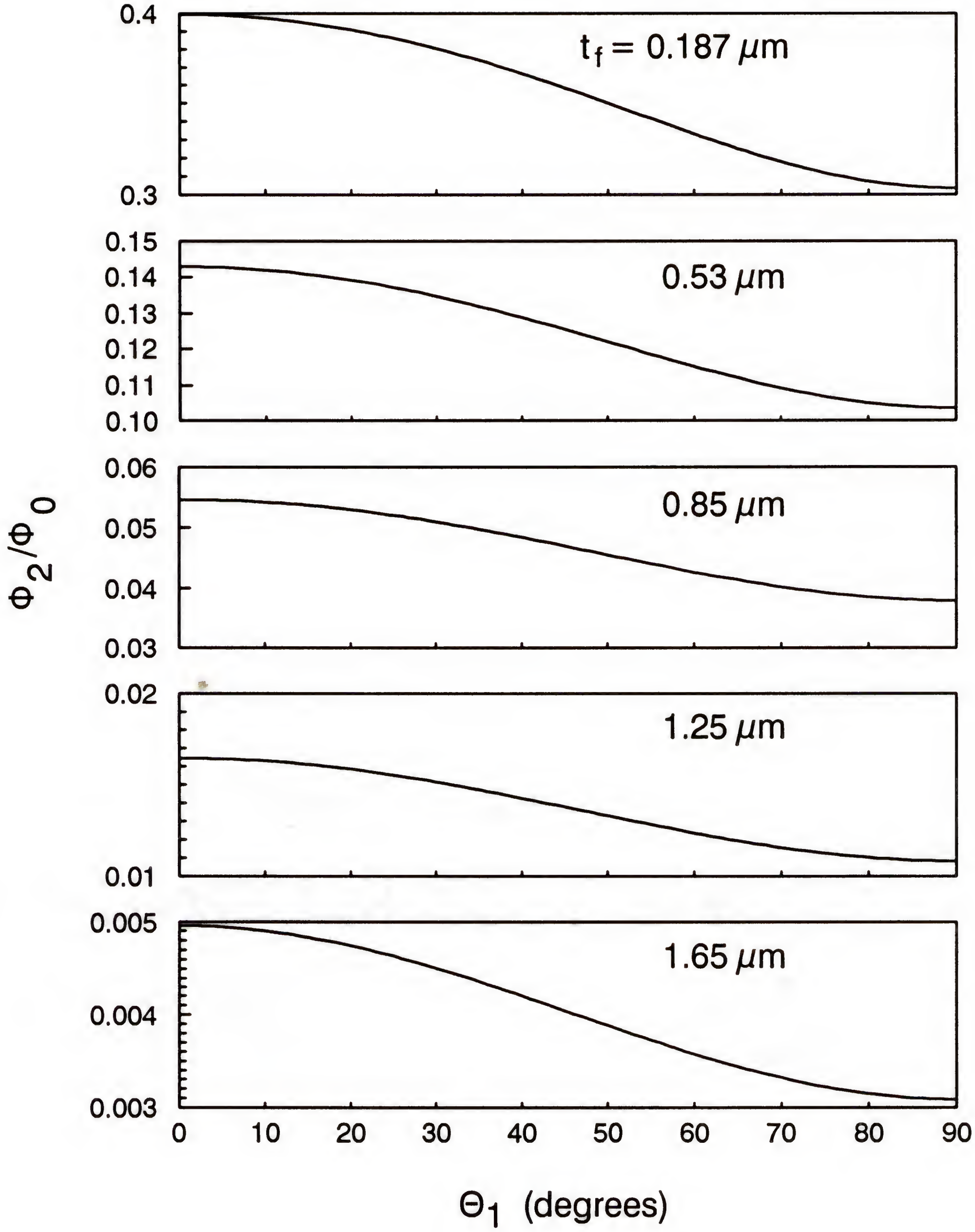


Figure 3.2 Ratio of ϕ_2/ϕ_0 calculated from Eq. (3.3) for different incident angles and Si film thicknesses.

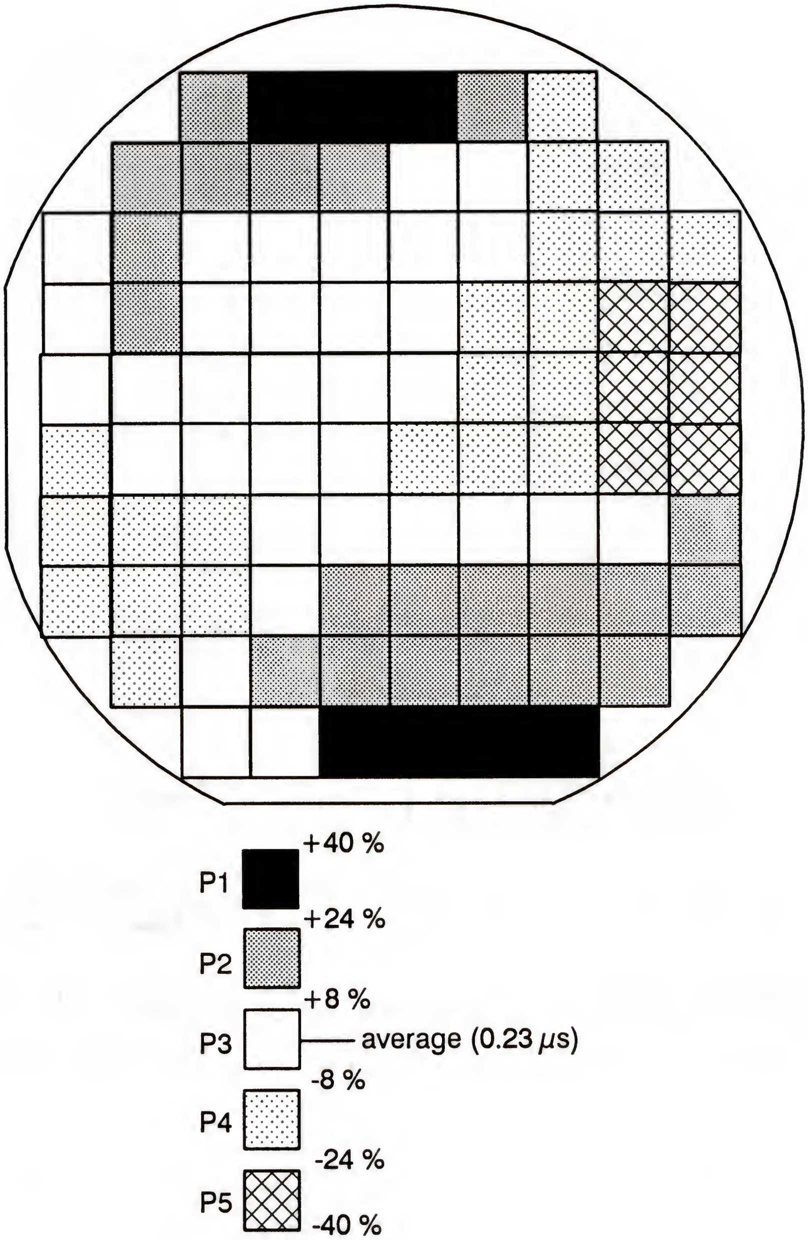


Figure 3.3 Mapping of τ_f in the SIMOX substrate for sample A1. The range of τ_f varies from 0.14 to 0.32 μs and the average value is 0.23 μs.

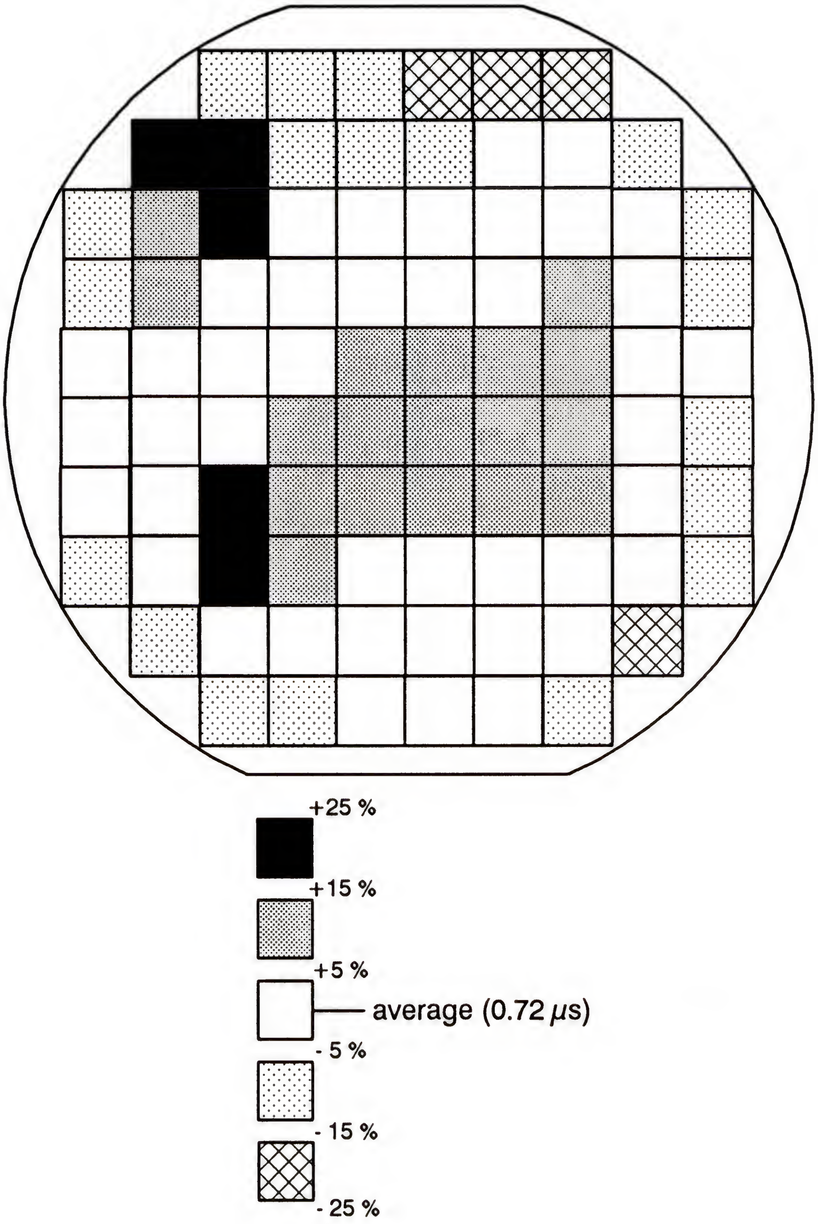


Figure 3.4 Mapping of τ_f in the SIMOX substrate for sample A5. The range of τ_f varies from 0.54 to 0.90 μs and the average value is 0.72 μs.

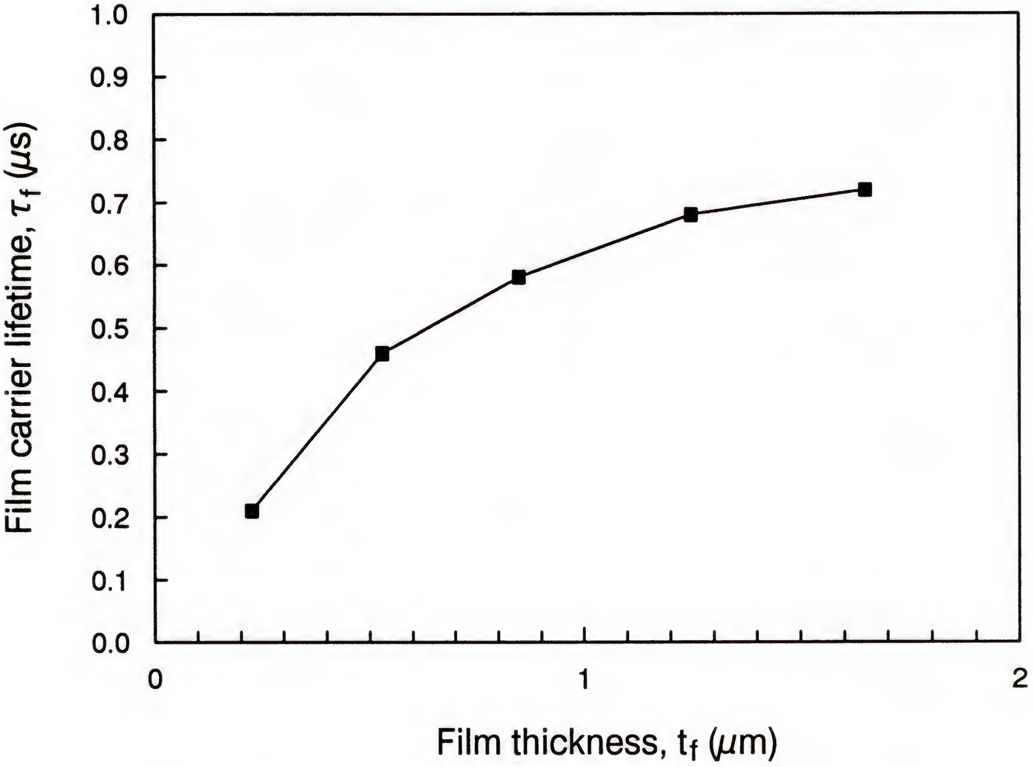


Figure 3.5 Film carrier lifetimes against film thicknesses for samples A1-A5 listed in Table 3.1.

CHAPTER 4
MEASUREMENTS OF INTERFACE STATE DENSITY IN PARTIALLY AND FULLY DEPLETED MOSFETs BY A HIGH-LOW-FREQUENCY (HLF) TRANSCONDUCTANCE METHOD

4.1 Introduction

Characterization of interface states in SOI (silicon-on-insulator) MOSFETs has been a subject of considerable interest. Due to the complex multi-interface nature and very small gate area of the SOI MOSFET's for VLSI circuit applications, it is difficult to determine the interface state properties by using the conventional capacitance and conductance methods. Several analytical models and characterization methods have been developed that correlate the dynamic transconductance and interface state admittance in SOI MOSFETs [70-73]. In these models, it is shown that the interface state density can be determined from the imaginary part of the transconductance measurements.

A new method has been proposed recently for determining the interface state density profile from the real part of the high-low-frequency (HLF) transconductance measurements on bulk Si MOSFETs [74]. Here, the high-low-frequency (HLF) transconductance method is applied to determine the interface state density profile in small-geometry thick- and thin-film (fully depleted) MOSFETs formed on single- and multiple-oxygen implanted (SIMOX) silicon substrates [75]. By comparing the real part of the measured high- and low-frequency transconductance and using a static drain current to gate voltage measurement on an MOSFET operating in the linear region, the energy distribution of the interface state density is determined without knowing the doping profile in the channel. Interface state densities determined by the

HLF transconductance method were found in good agreement with that determined by the charge pumping (CP) method.

4.2 Theory for the HLF Transconductance Technique

4.2.1 Thick-Film SOI MOSFETs

For an SOI MOSFET operating in the ohmic regime with grounded substrate and film thickness $t_f \geq 2x_{d(max)}$, where $x_{d(max)}$ is the maximum depletion-region width extending from an inverted surface [64], the drain current I_d is given by

$$I_d = \frac{W}{L}\mu_{\text{eff}} Q_i \cdot V_d \tag{4.1}$$

where W and L are the channel width and length, respectively, μ_{eff} is the effective mobility, Q_i is the absolute inversion layer charge, and V_d is the drain voltage. In weak inversion, Eq. (4.1) is valid for $V_d < kT/q$. By differentiating the drain current with respect to the gate voltage V_g, the transfer admittance is given by [70,73]

$$g_m = \frac{W C_i V_d}{L} \frac{\mu_{\text{eff}}^2}{\mu_0} \frac{C_{ox}}{C_{ox} + C_d + C_i + Y_{it}/j\omega} \tag{4.2}$$

where μ_0 is the low field mobility, C_{ox} is the gate oxide capacitance, C_d is the depletion layer capacitance, C_i is the inversion charge capacitance, Y_{it} is the interface state admittance, and ω is the angular frequency of the applied gate signal.

It has been shown that for an MOSFET with channel length smaller than 10 μm and operating in the weak inversion regime, the phase shift due to lateral transport of inversion carriers can be neglected up to frequencies much higher than that at which the interface states become totally inactive [70]. This argument implies that for such an MOSFET the delay in the inversion layer buildup is negligible. Therefore, C_i is independent of the small ac signal frequency and can be written as [70,76]

$$C_i = \frac{Q_i}{(kT/q)} \tag{4.3}$$

The transfer admittance in weak inversion is, therefore, given by

$$g_m = \frac{I_d}{(kT/q)} \frac{C_{ox}}{C_{ox} + C_d + C_i + Y_{it}/j\omega} \tag{4.4}$$

Equation (4.4) is obtained by assuming μ_{eff} equal to μ_0 in the weak inversion regime when the influence of surface potential fluctuation is neglected [70,73].

In the case of low-frequency ($\leq$ 10 Hz) operation, the interface state admittance may be approximated by

$$Y_{it} = G_{it} + j\omega C_{it} \tag{4.5}$$

where G_{it} and C_{it} denote the static interface state conductance and capacitance, respectively. It is noted that for ω=0, G_{it}=0 [71] and Y_{it}=$j\omega C_{it}$. By substituting Eq. (4.5) into Eq. (4.4), the real part of the inverse low-frequency transconductance can be expressed as

$$Re\left\{\frac{1}{g_m^{\text{LF}}}\right\} = \frac{(kT/q)}{I_d} \frac{C_{ox} + C_d + C_i + C_{it}}{C_{ox}} \tag{4.6}$$

In the case of high-frequency ($\geq$ 1 MHz) operation, the interface traps cannot follow the ac signal so that C_{it}=0 and the real part of the inverse high-frequency transconductance is given by

$$Re\left\{\frac{1}{g_m^{\text{HF}}}\right\} = \frac{(kT/q)}{I_d} \frac{C_{ox} + C_d + C_i}{C_{ox}} \tag{4.7}$$

From Eq. (4.6), Eq. (4.7) and the relation C_{it}=qD_{it}, the interface state density D_{it} can be expressed as [74]

$$D_{it} = \frac{I_d C_{ox}}{kT} \left[Re\left\{\frac{1}{g_m^{\text{LF}}}\right\} - Re\left\{\frac{1}{g_m^{\text{HF}}}\right\}\right] \tag{4.8}$$

and

$$E - E_i = qV_d + q\phi_B + kTln\left[\frac{I_d(V_g)}{I_d(V_{th})}\right] \tag{4.9}$$

Thus, D_{it} can be determined by measuring the high- and low-frequency transconductance and drain current. It is noted that the only device parameter required in Eq.

(4.8) is the oxide thickness, which can be determined with very good accuracy. By measuring I_d and V_{th} from an I_d versus V_g curve, values of $E - E_i$ are determined, and the relationship between D_{it} and $E - E_i$ can be established from Eqs. (4.8) and (4.9) without knowing the channel doping profile.

4.2.2 Thin-Film SOI MOSFETs

For a fully-depleted ($t_f \leq x_{d(max)}$) SOI MOSFET, the front- and back-gate voltages can be expressed as [77]

$$V_{gf} = V_{FB}^f + \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf} - \frac{C_b}{C_{of}}\psi_{sb} - \frac{Q_b/2 + Q_{cf} + Q_{itf}}{C_{of}} \tag{4.10}$$

and

$$V_{gb} = V_{FB}^b - \frac{C_b}{C_{ob}}\psi_{sf} + \left(1 + \frac{C_b}{C_{ob}}\right)\psi_{sb} - \frac{Q_b/2 + Q_{cb} + Q_{itb}}{C_{ob}} \tag{4.11}$$

where V_{FB}^f is the front-gate flatband voltage, C_b is the depletion capacitance, C_{of} is the front-gate oxide capacitance, ψ_{sf} is the front surface potential, Q_b is the depletion-region areal charge density, Q_{cf} is the front-surface areal carrier charge density, and Q_{itf} is the front Si/SiO$_2$ interface areal charge density. V_{FB}^b, C_{ob}, ψ_{sb}, Q_{cb}, and Q_{itb} are the back-gate counterparts of V_{FB}^f, C_{of}, ψ_{sf}, Q_{cf}, and Q_{itf}, respectively. When the back surface is accumulated, ψ_{sb} is virtually grounded, the transfer admittance in weak inversion for the front-gate transistor can be obtained by differentiating Eq. (4.10) with respect to ψ_{sf}, which yields [70,73]

$$g_{mf} = \frac{I_{df}}{kT/q}\frac{C_{of}}{C_{of} + C_b + C_{cf} + Y_{itf}/j\omega} \tag{4.12}$$

where I_{df} is the drain current of the front-gate transistor, $C_{cf}{=}-dQ_{cf}/d\psi_{sf}$ is the surface charge capacitance, and $Y_{itf}{=}-j\omega(dQ_{itf}/d\psi_{sf}){=}G_{itf}{+}j\omega C_{itf}$ is the interface-state admittance. From the measured I_{df}, high-frequency transconductance g_{mf}^{HF}, and low-frequency transconductance g_{mf}^{LF}, the interface state density D_{itf} of the front-gate Si/SiO$_2$ interface can be determined from Eq. (4.8).

In the case of accumulated back surface and dc operation, $d\psi_{sf}/dV_{gf}$ can be derived from Eq. (4.10), and the result is

$$\frac{d\psi_{sf}}{dV_{gf}} = \frac{C_{of}}{C_{of} + C_b + C_{cf} + C_{itf}} \tag{4.13}$$

Now solving Eqs. (4.12) and (4.13), we obtain

$$\frac{d\psi_{sf}}{dV_{gf}} = \frac{(kT/q)}{I_{df}} \frac{1}{Re\left\{\frac{1}{g_{mf}^{\mathrm{LF}}}\right\}} \tag{4.14}$$

For the dc case $dV_{gf}/dI_{df} = Re\left\{\frac{1}{g_{mf}^{\mathrm{LF}}}\right\}$, the surface potential can be expressed in terms of I_{df} by integrating Eq. (4.14) from threshold voltage V_{thf} to V_{gf}. Thus, by expressing ψ_{sf} in terms of energy (E) relative to the intrinsic Fermi energy (E_i), Eq. (4.14) is reduced to Eq. (4.9).

It should be noted that the above analysis can be applied equally well for characterizing the interface state density of the back-gate Si/SiO$_2$ interface provided that the derivation is from Eq. (4.11) with the front-surface in accumulation.

4.3 Results and Discussion

High-low-frequency transconductance measurements were made on single- and multi-implanted thick-film SIMOX n-channel enhancement-mode MOSFETs with channel length of 2.5 μm and width of 50 μm. The doping concentration under the gate oxide (325Å) is about 5×10^{16} cm^{-3} as shown in Table 4.1. The former is prepared by single oxygen implant to a dose of 1.5×10^{18} cm^{-2} followed by annealing at 1285 °C for 2 hours. The latter is prepared by multiple oxygen implants to a total dose of 1.6×10^{18} cm^{-2} with each implant dose of 4×10^{17} cm^{-2} and annealed at 1285 °C for 2 hours. The multiple implantation process is known to produce SIMOX substrates of very high quality [78]. Table 4.2 lists the material parameters of the thin-film SIMOX samples used in our study. The n-channel (N1, N2) and p-channel (P1, P2) enhancement-mode MOSFETs have a channel length of 1.8 μm, width of

3.6 μm, gate oxide of 200 $\mathring{A}$, buried oxide of 3900 $\mathring{A}$, and film doping concentration of 1×10^{16} cm^{-3}.

The HLF transconductance measurements were performed at frequencies of 1 MHz and 10 Hz using an HP 4192A impedance analyzer with drain voltage kept at 25 mV and 20 mV for the thick-film and thin-film MOSFETs, respectively. Figure 4.1 shows the experimental set up used in this study.

Figure 4.2 shows the transconductance versus gate bias for the single- (SI) and multi-implanted (MI) SIMOX MOSFETs listed in Table 4.1. The transconductance curves of the multi-implanted sample are shifted horizontally for clarity. The inset in Fig. 4.2 shows Δg_m ($\equiv Re\{g_m^{\mathrm{HF}}\} - Re\{g_m^{\mathrm{LF}}\}$) versus gate voltage. It is clearly shown that the difference between the high- and low-fequency transconductance is smaller for the multi-implant sample, which implies a lower interface state density.

Figure 4.3 shows the distribution of interface traps in the forbidden gap determined from Eqs. (4.8) and (4.9) for both the SI and MI samples. The result is valid only in a limited energy range of the forbidden gap. This range extends from the onset of weak inversion to the onset of strong inversion ($V_g = V_{th}$). The results show that the interface state density near midgap can be reduced by using a multi-implant process to the same value as bulk Si MOSFETs [74]. Thus, the multi-implant approach may be favorable for SIMOX technology.

Figure 4.4 through Fig. 4.7 show the measured I-V and the high- and low-frequency transconductance of sample N1 and P1 at back-gate biases V_{gb}=-1, -5, and -10 V for the n-channel and 1, 5, and 10 V for the p-channel devices, respectively. The voltage V_{gb}^A, required to make the back-gate accumulated and $\psi_{sb} \approx 0$, is determined from the I-V measurements under different back-gate biases. The values are $V_{gb}^A \approx -6$ and 6.5 V for the n- and p-channel MOSFETs, respectively. It is noted that the shift in I_{df} vs. V_{gf} curve shown in Figs. 4.4 and 4.5 and $Re\{g_{mf}\}$ vs. V_{gf} curve shown in Figs. 4.6 and 4.7 are due to the change of threshold voltage for different back-gate biases [77]. The distribution of interface state density calculated from the results of Figs. 4.4 through 4.7 at $V_{gb} = -10$ V for n-channel and +10 V for p-channel devices are shown in Fig. 4.8.

In order to compare the results of the HLF transconductance method with existing methods, we have also performed the charge pumping (CP) measurements on these devices. The results for samples SI and MI are shown in Fig. 4.9. The interface states density was calculated from the measured charge pumping current I_{cp} by [79,80]

$$I_{cp} = f.A_G.q^2.\overline{D_{it}}.\Delta\psi_s \tag{4.15}$$

where f is the repetitive pulse frequency, A_G is the channel area of the MOSFET (cm^2), $\overline{D_{it}}$ is the mean interface state density (cm$^{-2}eV^{-1}$), $\Delta\psi_s$ is the total sweep of the surface potential, and q is the electronic charge. The interface state densities determined by the charge pumping method for samples SI and MI are also shown in Fig. 4.3. Reasonable agreement was obtained between these two methods. It is noted that at least ten samples for each structure were measured by the HLF transconductance method. The results are summarized in Table 4.1 and Table 4.2.

4.4 Conclusion

In conclusion, we have demonstrated that the modified HLF transconductance method can be applied to both thick- and thin-film SOI MOSFETs formed on SIMOX substrates. We have determined the interface state density profile in the band gap from the real part of the measured HLF transconductance and the surface potential from the measured static drain current versus gate voltage curve. We have successfully demonstrated that the HLF transconductance method can be used in the characterization of front- and back-gate channel interface state density for the fully depleted SOI MOSFETs.

Table 4.1 Device parameters and measured interface state densities in thick-film SOI MOSFET's formed on SIMOX substrates.

Sample	SIMOX Dose	SIMOX Anneal	Film Thickness	Midgap D_{it} ($\times 10^{10}$ cm^{-2}eV^{-1}) (HLF), (CP)
Single-implantation (SI)	1.5E18 cm^{-2} 200 keV 600 °C	1285 °C 2 hr.	0.5 μm	7.6±0.6, 7.2±0.4
Multi-implantation (MI)	4×4E17 cm^{-2} 150 keV 550 °C	4×1285 °C 2 hr.	0.5 μm	2.2±0.5, 1.8±0.4

Table 4.2 Device parameters and measured interface state densities in thin-film SOI MOSFET's formed on SIMOX substrates. The SIMOX substrate are formed by implanting oxygen dose 1.8×10^{18} cm^{-2} and annealing at 1310 °C for 5 hours.

Sample	W/L (μm)	Film Thickness (μm)	Midgap D_{it} ($\times10^{10}$ $cm^{-2}eV^{-1}$) (HLF) (front-gate, back-gate)	Midgap D_{it} ($\times10^{10}$ $cm^{-2}eV^{-1}$) (CP) (front-gate)
N1	3.6/1.8	0.28	6.0±0.6, 8.8±0.6	5.2±0.3
P1	3.6/1.8	0.28	8.5±0.5, 10.5±0.6	7.4±0.3
N2	50/1.5	0.11	7.5±0.4, 9.0±0.5	6.3±0.4
P2	50/1.5	0.11	9.3±0.5, 11.0±0.5	8.0±0.4

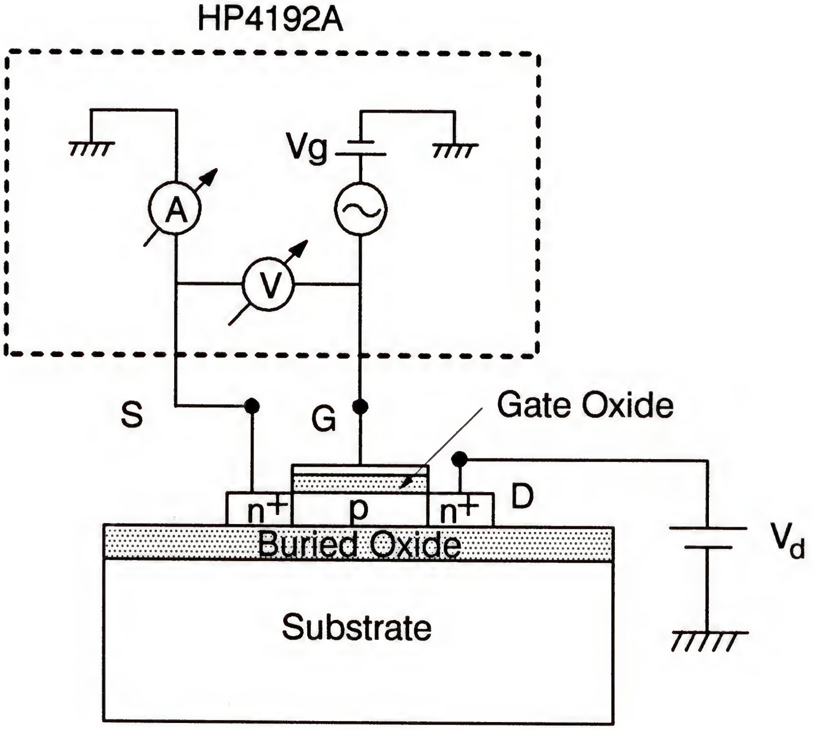


Figure 4.1 Schematic diagram of the experimental setup for the SOI MOSFETs transconductance measurements [70].

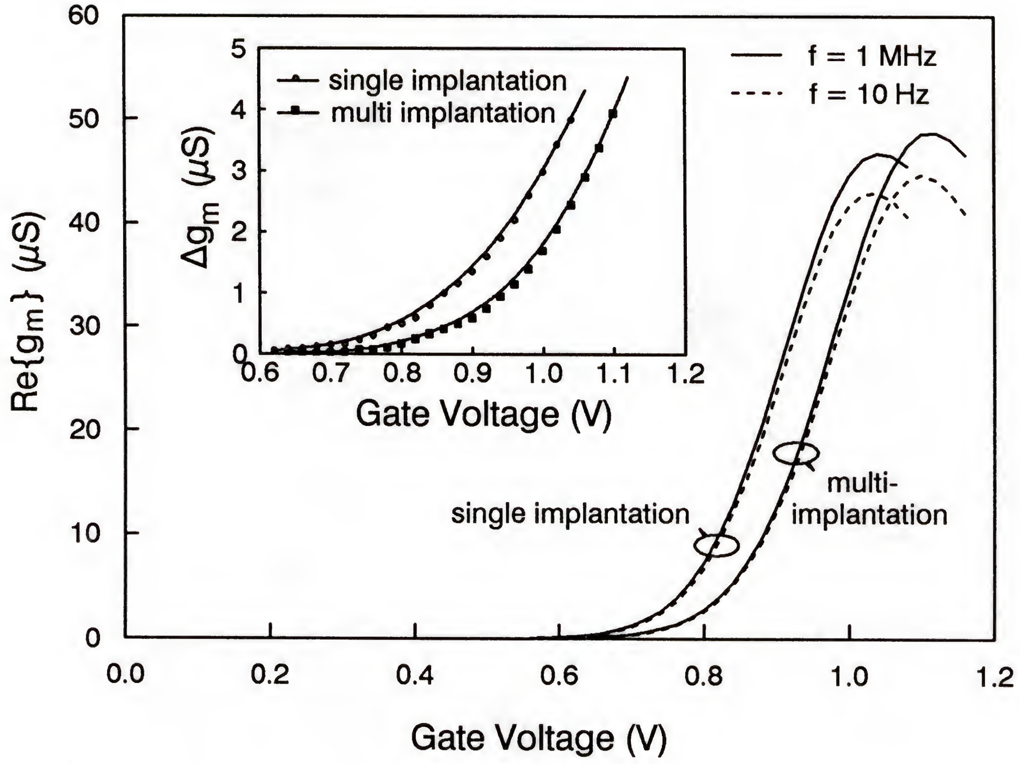


Figure 4.2 High- and low-frequency transconductances versus gate bias for single- (S1) and multi-implanted (M1) SOI MOSFETs. The inset shows the difference between the high- and low-frequency transconductance ($\Delta g_m \equiv Re\{g_m^{\mathrm{HF}}\} - Re\{g_m^{\mathrm{LF}}\}$) versus gate voltage.

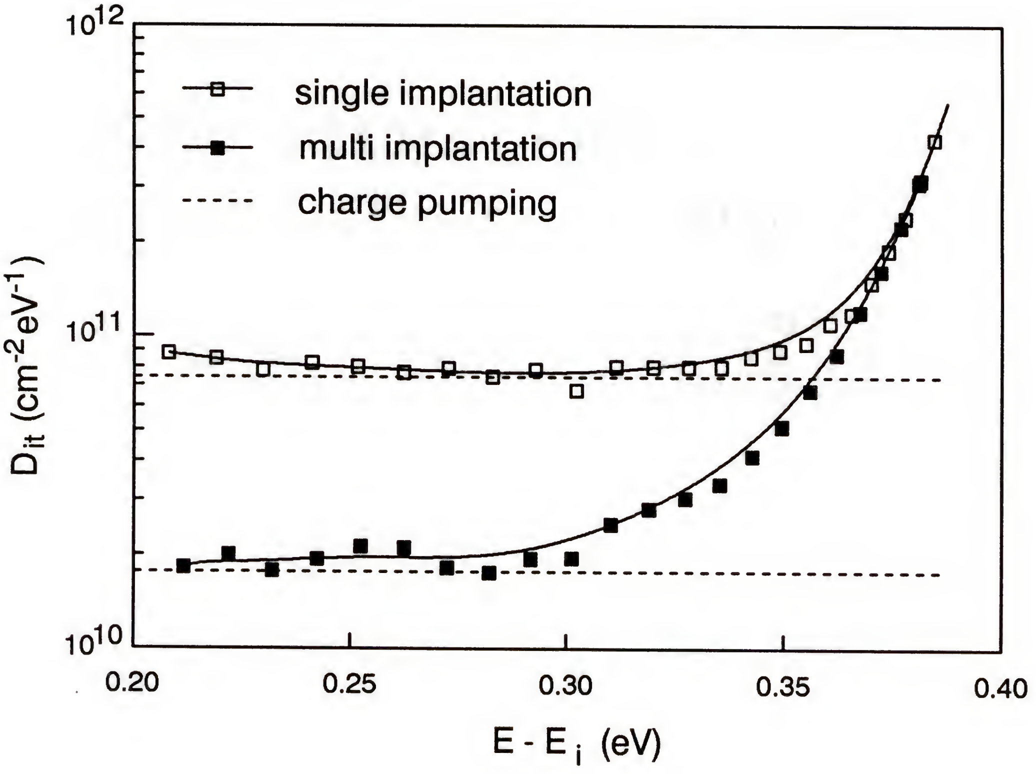


Figure 4.3 Interface state density D_{it} versus energy (relative to the intrinsic Fermi energy E_i) of the single- and multi-implanted SOI MOSFETs determined by the high-low-frequency transconductance and charge pumping methods.

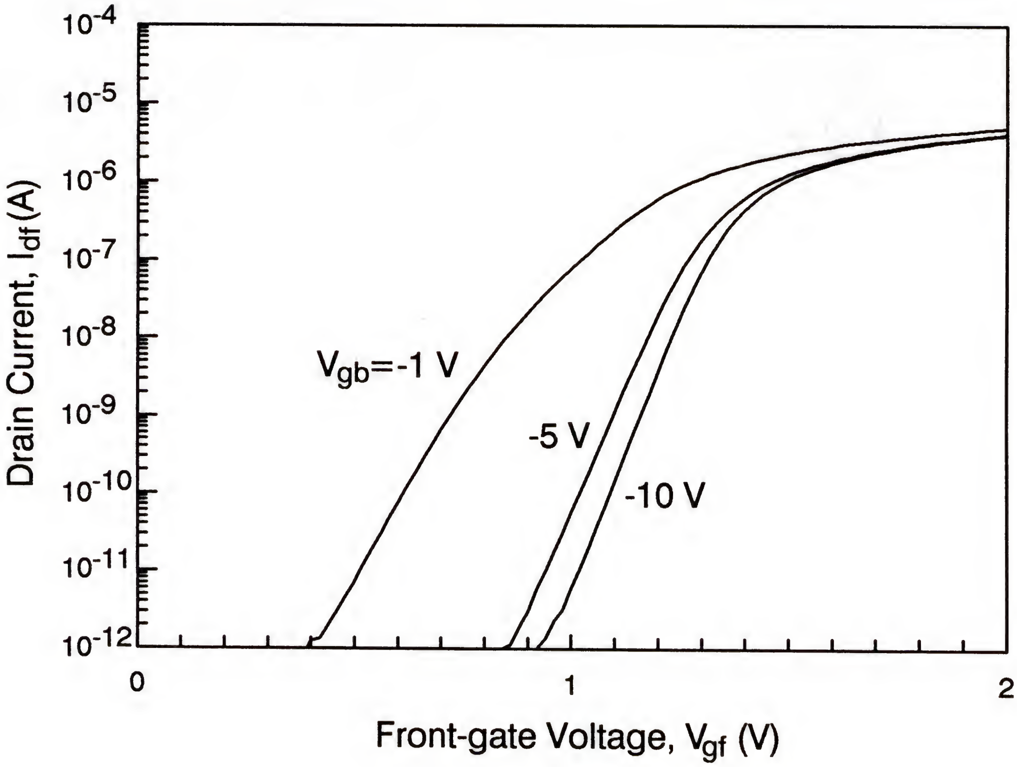


Figure 4.4 Drain current versus front-gate voltage for sample N1 at back-gate biases of −1, −5, and −10 V, respectively.

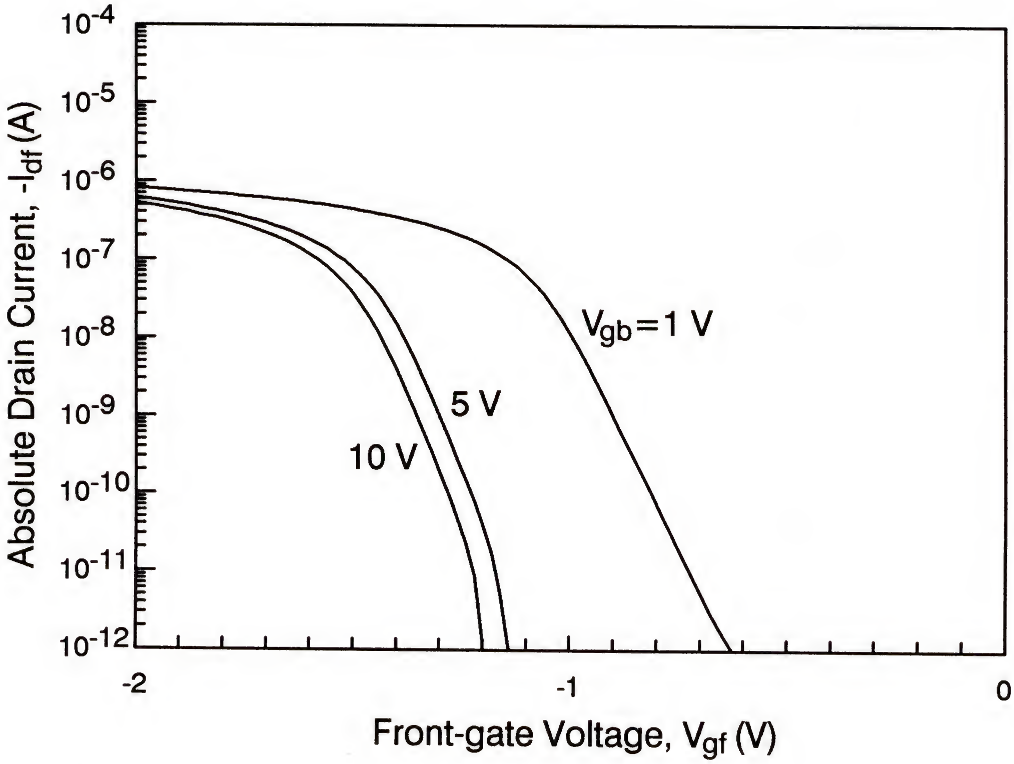


Figure 4.5 Drain current versus front-gate voltage for sample P1 at back-gate biases of 1, 5, 10 V, respectively.

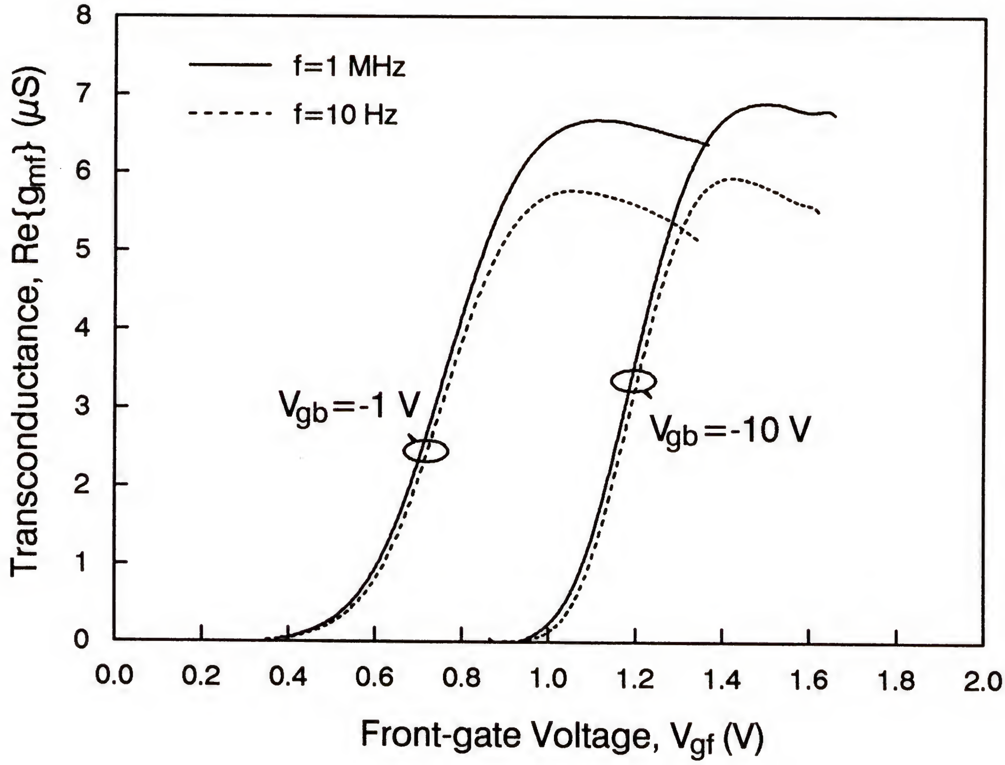


Figure 4.6 High- and low-frequency transconductances versus front-gate voltage for sample N1 at back-gate biases of -1 and -10 V, respectively.

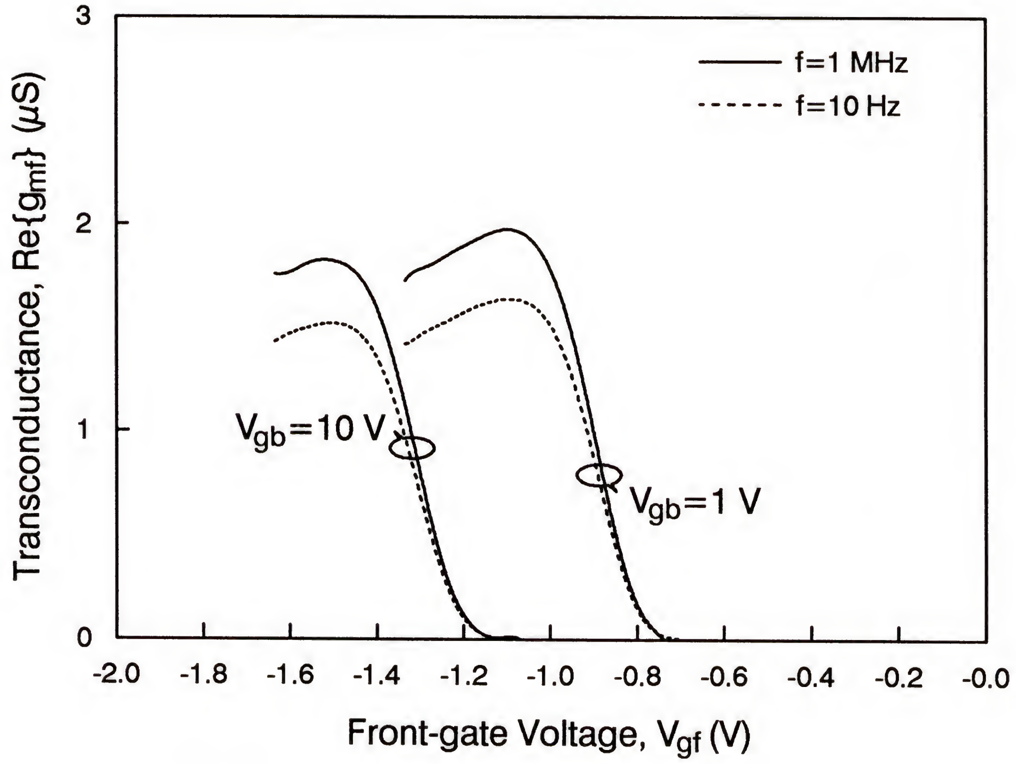


Figure 4.7 High- and low-frequency transconductances versus front-gate voltage for sample P1 at back-gate biases of 1 and 10 V, respectively.

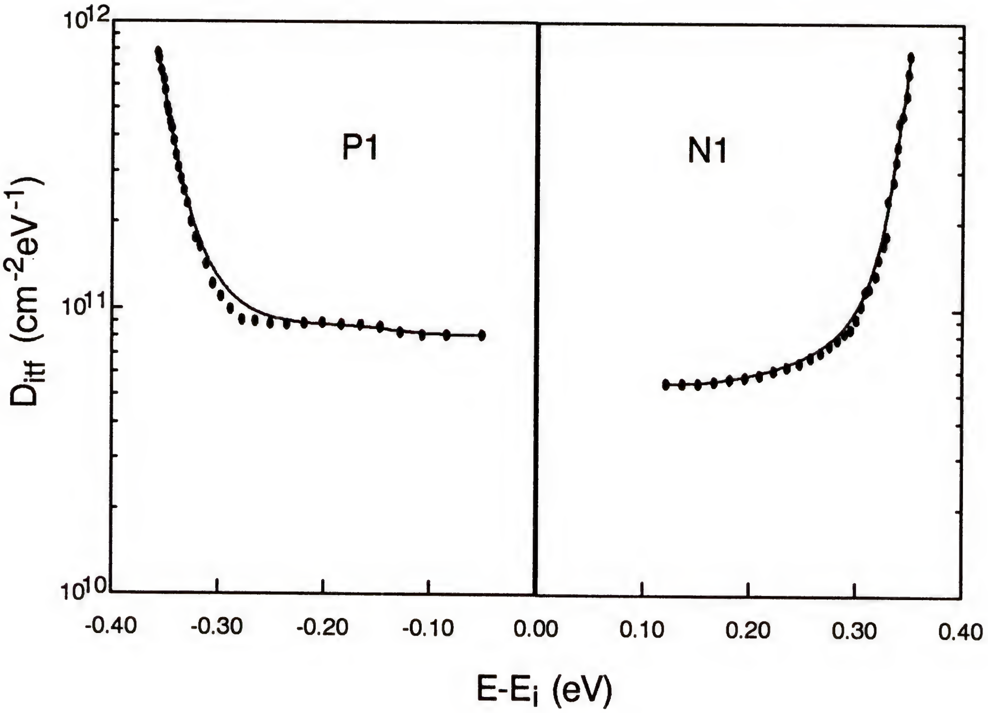


Figure 4.8 Interface state density D_{itf} at the front-gate Si/SiO$_2$ interface versus energy of the forbidden gap, determined by high-low-frequency transconductance method for sample N1 at a back-gate bias of -10 V and sample P1 at a back-gate bias of 10 V, respectively.

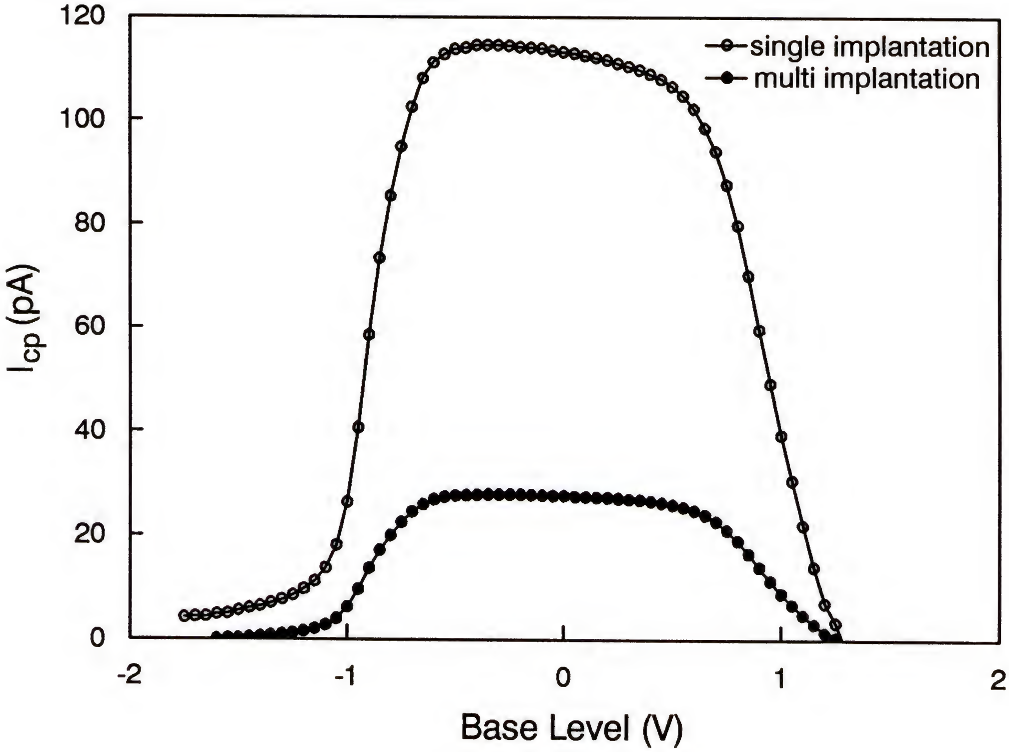


Figure 4.9 Measured charge pumping curves for the single- and multi-implanted SOI MOSFETs. The charge pumping conditions are: V_r=0.1 V, ΔV_A=4 V, f=10 KHz.

CHAPTER 5
INTERFACE CHARACTERIZATION OF FULLY DEPLETED SOI MOSFETs BY A THRESHOLD VOLTAGE METHOD

5.1 Introduction

Determination of the interface state density profile in a fully-depleted SOI MOSFET has been a subject of interest in recent years. Due to the ultra-thin (fully depleted) film nature of the SOI (silicon-on-insulator) structure, the electrical properties of SOI MOSFETs are influenced by the charge coupling between the front- and back-gate. The capacitance and conductance methods are difficult for characterizing interface state density because of the complex multi-interface and the large film series resistance problems in an SOI MOSFET. Recently, charge pumping and dynamic transconductance techniques have been used for characterizing interface states in the SOI MOSFETs [55,56]. Using these techniques, it is shown that the interface state density can be determined by measuring the imaginary part or real part (discussed in Chapter 4) of the transconductance.

Since the threshold voltage of an SOI MOSFET is sensitive to the interface states and gate bias, it is possible to determine the interface state density profile from the threshold voltage measurements. In this chapter, we report a new threshold voltage technique for determining the interface state profile in a fully depleted SOI MOSFET operating in the linear region. By measuring threshold voltage of the front-gate under different back-gate bias conditions, the back-gate interface state profile can be determined. The front-gate interface states can be characterized in a similar way by reversing the polarity of the bias across the gates. The main advantage of this method is the simplicity of the threshold voltage measruements which eliminate the problems associated with the dynamic transconductance techniques.

5.2 Theory for Threshold Voltage Method

When the back surface of an SOI MOSFET is depleted, the threshold voltage of the front-gate can be written as [77]

$$V_{Tf} \approx V_{Tf}^A - \frac{C_b C_{ob}}{C_{of}(C_b + C_{ob} + C_{itb})}(V_{Gb} - V_{Gb}^A) \tag{5.1}$$

where V_{Gb} is the back-gate voltage, V_{Tf}^A denotes the front-gate threshold voltage when $V_{Gb}{=}V_{Gb}^A$, V_{Gb}^A is the back-gate voltage when the back-surface is in accumulation, C_b is the depletion capacitance, C_{of}, C_{ob} are the front-gate and back-gate oxide capacitances, respectively, and $C_{itb}{=}qD_{itb}$ is the capacitance associated with the back-gate interface trap charge. By rewriting Eq. (5.1), we obtain

$$D_{itb} = -\frac{1}{q}\left[\left(\frac{C_b C_{ob}}{C_{of}}\right)\frac{dV_{Gb}}{dV_{Tf}} + C_b + C_{ob}\right] \tag{5.2}$$

From Eq. (5.2), D_{itb} can be deduced from the measured V_{Tf}. It is noted that the device parameters required for calculating D_{itb} are the thickness of top Si film, the front- and back-gate oxides, which can be determined with very good accuracy [81-83].

For a strongly inverted front surface, the back surface potential ψ_{sb} versus V_{Gb} can be expressed by [77]

$$V_{Gb} = V_{Gb}^A - \frac{C_b}{mC_{of}}\psi_{sb} \tag{5.3}$$

where $m = dV_{Tf}/dV_{Gb} = -C_b C_{ob}/C_{of}(C_b + C_{ob} + C_{itb})$ is dependent on V_{Gb}. By expressing ψ_{sb} in terms of energy (E) relative to the intrinsic Fermi energy (E_i), we have

$$E - E_i = -\frac{qmC_{of}}{C_b}(V_{Gb} - V_{Gb}^A) - q\phi_B \tag{5.4}$$

where ϕ_B is the film-body Fermi potential. Thus, the relationship between D_{itb} and $(E - E_i)$ can be established using Eqs. (5.2) and (5.4).

It should be noted that the above analysis can be applied equally well for characterizing the interface trap charge density of the front-gate Si/SiO$_2$ interface by reversing the polarity of bias voltages applied to the front- and back-gate of the SOI MOSFETs.

5.3 Results and Discussion

The threshold voltage method was applied to an n-channel SOI MOSFET with channel length of 1.8 μm, width of 2.4 μm, gate oxide of 150 $\AA$, buried oxide of 3500 $\AA$, film thickness of ~1200 $\AA$, and film doping concentration of $\sim 4\times 10^{16}$ cm^{-3}. Static drain current measurements were performed using an HP4145B semiconductor parameter analyzer. The relation between the drain current (I_{Df}) and the threshold voltage (V_{Tf}) of the front gate under strong-inversion in the linear region [$V_{Df} \ll (V_{Gf} - V_{Tf})$] can be expressed by [64,77]

$$I_{Df} \simeq \frac{Z}{L}\mu_{nf}C_{of}(V_{Gf} - V_{Tf})V_{Df} \tag{5.5}$$

where Z is the channel width, L is the channel length, and μ_{nf} is the low-field mobility. In Eq. (5.5), the series resistance and mobility degradation effects are neglected due to θ, $\alpha_R \ll 1$ [84]. Equation (5.5) shows that the threshold voltages can be determined from the linear extrapolation of the measured I_{Df}-V_{Gf} curve to the V_{Gf} axis. It is noted that the threshold voltage determined in this way is independent of the surface potential ψ_{sf} for the threshold condition [85].

Figure 5.1 shows the I_{Df}-V_{Gf} plots at various back-gate voltages. Although small deviation exists at higher front-gate voltages, the linear relation are observed (as predicted by Eq. (5.5)) for $V_{Df} + V_{Tf} \ll V_{Gf} < \sim 1.5$ V in the present case. The points of maximum slope on the I_{Df}-V_{Gf} curves as found in the maximum transconductance values ($g_m = \partial I_{Df}/\partial V_{Gf}$ in Fig. 5.2) are also shown in Fig. 5.1. By making tangential lines to the curves at the maximum transconductance points and extrapolating to the curve I_D=0, the threshold voltages V_{Tf} can be determined. It should be noted that the threshold voltage cannot be determined from $I_{Df}(V_{Gf})$ characteristic curve if the back-channel current is significant for the back-surface inversion.

Fiqure 5.3 shows that the measured threshold voltage is a linear function of V_{Gb} when the back-surface is depleted (*i.e.*, $V_{Gb}^A < V_{Gb} \leq 0$ V). For $V_{Gb} < V_{Gb}^A$, V_{Tf} is equal to V_{Tf}^A, and is independent of V_{Gb}. Therefore, the back-gate voltage V_{Gb}^A for the back-surface accumulation can be determined from the intersection of the lines fitting the data in regions (I) and (II) as shown in Fig. 5.3.

Figure 5.4 shows the distribution of the interface state density in the band gap for the fully depleted SOI MOSFETs as determined from Eqs. (5.2) and (5.4) using threshold voltage method. In the calculation of D_{itb} in Eq. (5.2), dV_{Gb}/dV_{Tf} is approximated by $\Delta V_{Gb}/\Delta V_{Tf}$ with ΔV_{Gb}=0.1 V. The result is accurate from near midgap in depletion to near valence-band edge in accumulation. In the present case, the back-gate interface state density (D_{itb}) was found to be around 1.5×10^{11} $\text{cm}^{-2}\cdot\text{eV}^{-1}$ near midgap. By interchanging the role of the front- and back-gate, the front-gate interface state density (D_{itf}) was found to be $\sim 6\times10^{10}$ $\text{cm}^{-2}\cdot\text{eV}^{-1}$ near midgap. It should be noted that D_{itf} is less accuracy than D_{itb} determined by this method since $C_{of} > C_{ob}$ generally.

5.4 Conclusion

In summary, we have demonstrated a new threshold voltage technique for characterizing the interface properties of a fully depleted SOI MOSFET operating in the linear region. It is shown that using a simple static drain current measurement, both the front- and back-gate interface state density profiles of SOI MOSFETs can be determined from the threshold voltage method.

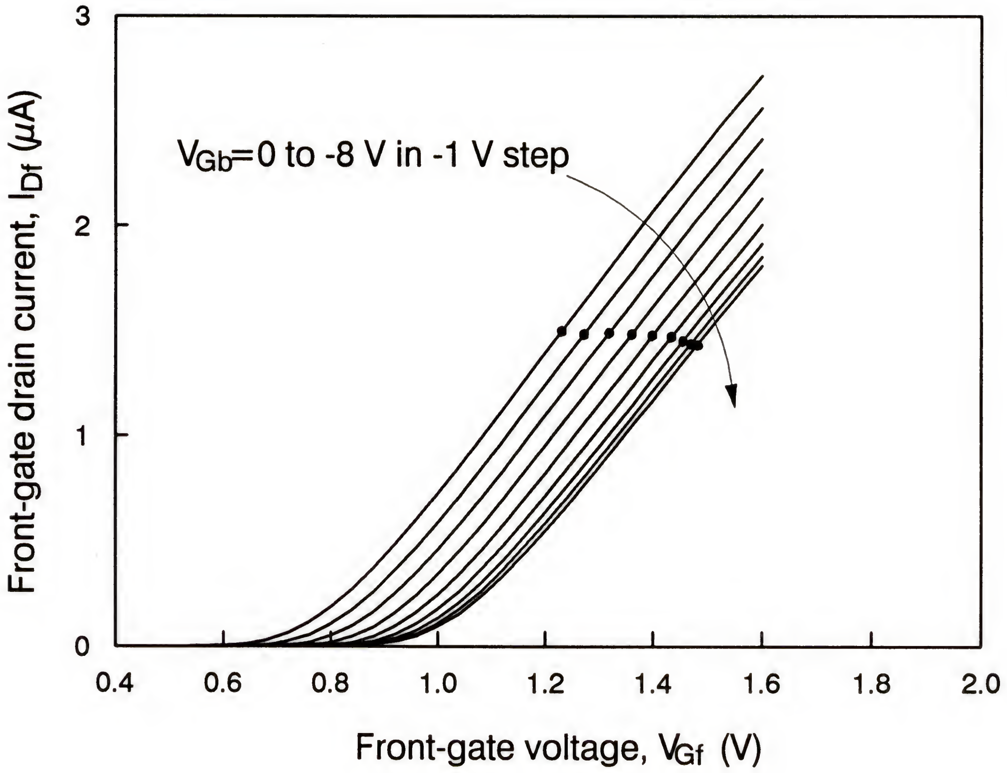


Figure 5.1 The measured front-channel drain current I_{Df} versus front-gate voltage V_{Gf} for different back-gate bias voltages (V_{Gb}=0 to -8 V in -1 V step). From linear extrapolation of these curves to V_{Gf} axis, the threshold voltage can be determined.

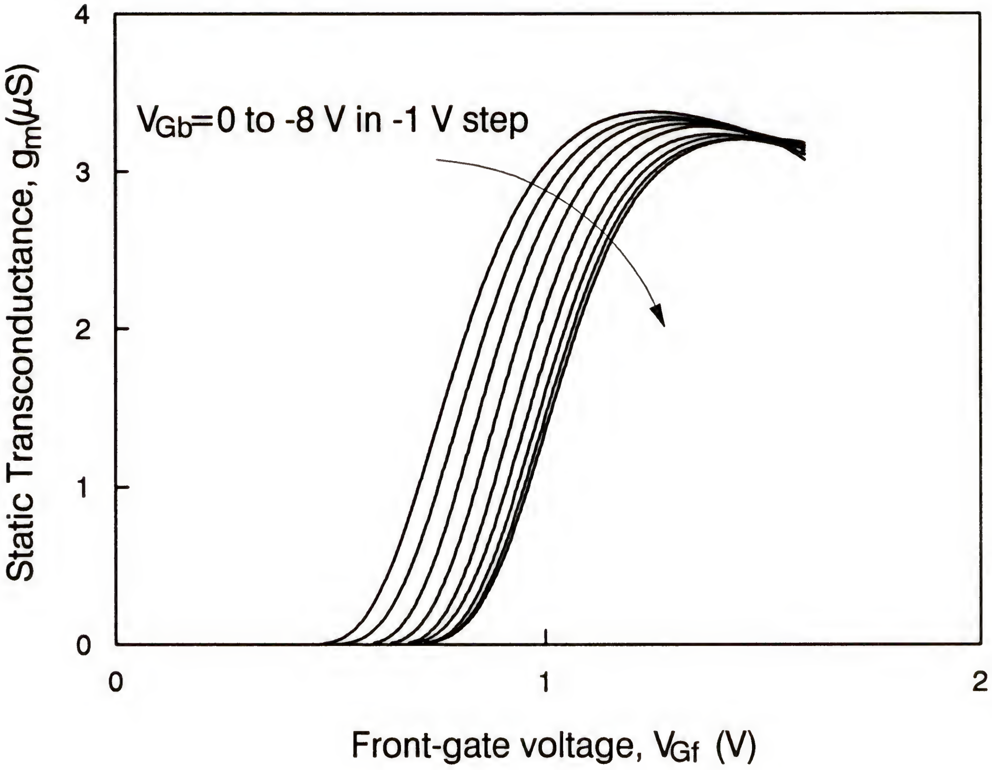


Figure 5.2 Measured static transconductance $g_m = \partial I_{Df}/\partial V_{Gf}$ versus front-gate voltage V_{Gf} for different back-gate bias voltages (V_{Gb}=0 to -8 V in -1 V step). The points of maximum slope for the curves in Fig. 5.1 are obtained from the maximum transconductance values of these curves.

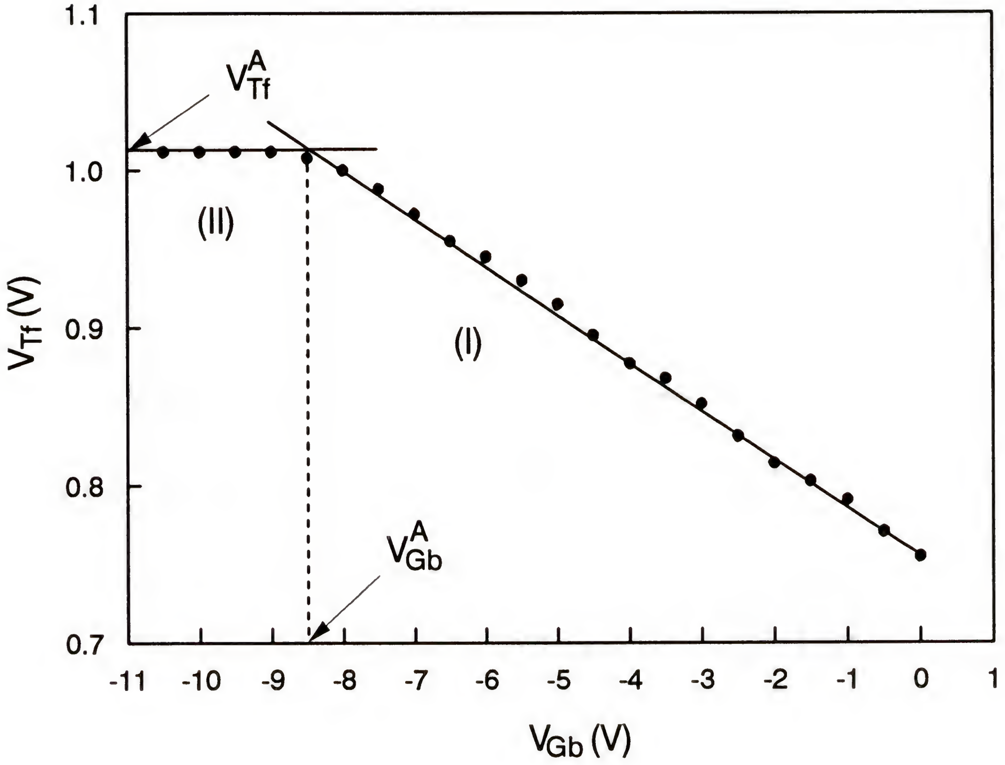


Figure 5.3 Front-gate threshold voltage V_{Tf} versus back-gate voltage V_{Gb} as determined from Fig. 5.1.

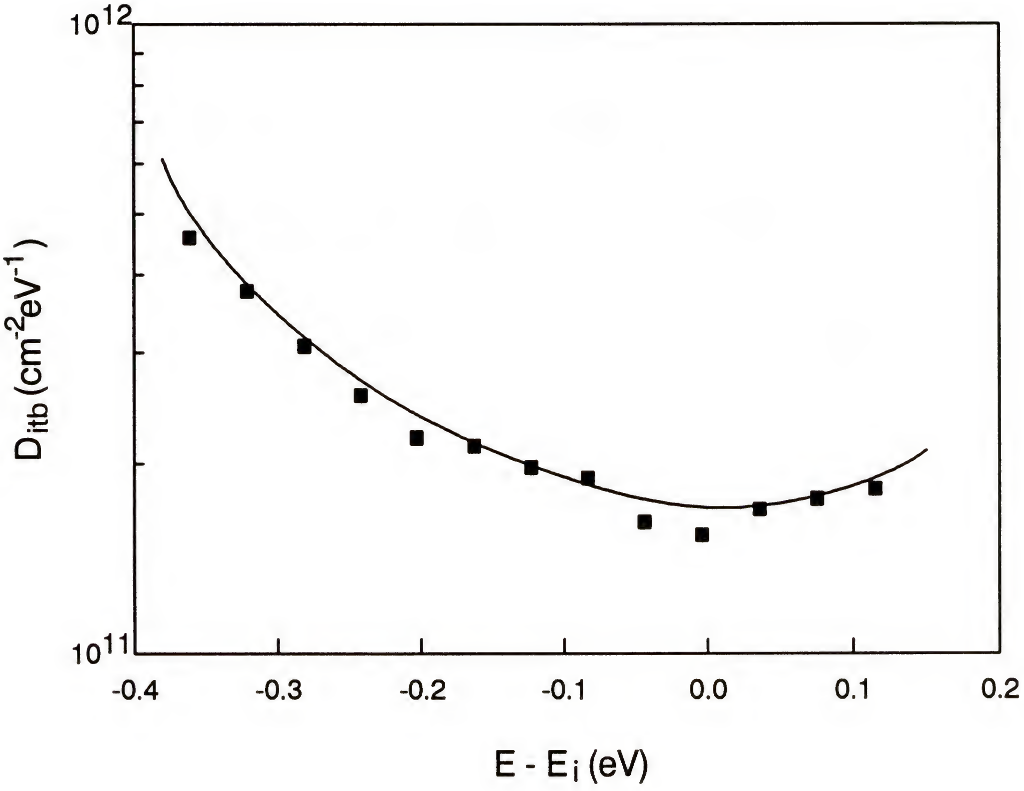


Figure 5.4 Interface state density D_{itb} at the back-gate Si/SiO$_2$ interface versus energy E (relative to the intrinsic Fermi energy E_i) in the forbidden gap, as determined by the threshold voltage method for samples described in the text.

CHAPTER 6
ANALYSIS OF CURRENT-VOLTAGE CHARACTERISTICS FOR FULLY DEPLETED SOI MOSFETs

6.1 Introduction

The advantages of improved isolation, reduced parasitics, and increased radiation hardness have promoted the development of thin-film (fully depleted) silicon-on-insulator (SOI) technology and stimulated interest in modeling the thin-film SOI MOSFET. The characteristics of thin-film SOI MOSFETs differ from the bulk counterparts due to effects of the charge coupling between the front and back gates. Several models that account for the structural uniqueness of the device have been reported [86-92]. In strong inversion, the approximation of current-voltage characteristics for thin-film SOI MOSFETs is given by Lim and Fossum [86]. The ideas of the long-channel MOSFET model [93] for bulk MOSFET, which are valid for all regions of operation, including the subthreshold regime and the saturation regime, suggest the possibility of developing a similar model for fully depleted SOI MOSFETs.

In this chapter we present an analytic model for fully depleted SOI MOSFETs, which contains the dependence of current-voltage characteristics on the front gate-source, back gate-source, and drain-source potentials. In the analysis, a complete depletion of the film body is assumed and the inversion charge density is related to the front surface potential by the theories developed for bulk and SOI MOSFETs. The analysis, which is valid for back surface depletion and accumulation, describes correctly the threshold voltage, the drain current, and the conductances in all regions of operation. The charge-sheet model and strong-inversion assumption are contained and considered approximations in this model.

6.2 Surface Potential and Threshold Voltage

Consider a fully depleted n-channel SOI MOSFET as shown in Fig. 6.1. The carrier densities in the silicon film are given by

$$p = N_A exp(-\beta\psi) \tag{6.1}$$

$$n = \frac{n_i^2}{N_A} exp\{\beta[\psi - V(y)]\} \tag{6.2}$$

where $\beta = q/kT$, $V(y)$ is the voltage drop along the channel. By integrating the Poisson's equation in the x direction, the free carrier charge density at each point y along the channel can be obtained as [64,93]

$$Q_{nf} = Q_s - Q_D \tag{6.3}$$

where

$$Q_s = -\lambda C_{of} \left\{ \psi_{sf} - \psi_{sb} + \frac{1}{\beta}\{exp(-\beta\psi_{sf}) - exp(-\beta\psi_{sb}) + exp[\beta(\psi_{sf} - 2\phi_B - V)]\} \right.$$
$$\left. - \frac{1}{\beta} exp[\beta(\psi_{sb} - 2\phi_B - V)] \right\}^{1/2}, \tag{6.4}$$

and

$$Q_D = -\lambda C_{of}(\psi_{sf} - \psi_{sb})^{1/2} \tag{6.5}$$

In Eqs. (6.4) and (6.5), $\lambda = (2\epsilon q N_A)^{1/2}/C_{of}$, $\phi_B = \beta^{-1} ln(N_A/n_i)$, and ψ_{sf} and ψ_{sb} represent the front and back potentials, respectively. It should be noted that Eq. (6.3) is valid for a depleted or accumulated back surface where the inversion charge density is negligible [77]. From the one-dimensional charge-coupling analysis that applies Gauss's law to the front and back SiO_2 interfaces, the inversion (electron) charge density can be written as [77]

$$Q_{nf} = -C_{of}\left[V_{Gf} - V_{FB}^{f} - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf} + \frac{C_b}{C_{of}}\psi_{sb} + \frac{Q_b}{2C_{of}}\right] \tag{6.6}$$

where $Q_b = -qN_At_b$ is the depletion-region areal charge density. The symbols in Eq. (6.6) have their usual meanings. The relationship between ψ_{sf} and $V(y)$ can be obtained from Eqs. (6.3) and (6.6). Before we proceed, it is interesting to discuss the following two approximations:

1. *When the front surface is strongly inverted*, Eq. (6.4) can be approximated by [93]

$$Q_s \approx -\lambda C_{of} \left\{ \frac{1}{\beta} exp[\beta(\psi_{sf} - 2\phi_B - V)] \right\}^{1/2} \tag{6.7}$$

By solving Eqs. (6.3), (6.6) and (6.7), the front surface potential is then given by

$$\psi_{sf}(y) = 2\phi_B + V(y) + \frac{1}{\beta} ln(\beta V_x^2/\lambda^2) \tag{6.8}$$

where

$$V_x = V_{Gf} - V_{FB}^f - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf} + \frac{C_b}{C_{of}}\psi_{sb} + \frac{Q_b - 2Q_D}{2C_{of}} \tag{6.9}$$

2. *When the front surface is depleted or weakly inverted*, the inversion charge density in Eq. (6.6) approaches zero. This gives

$$\psi_{sf} = \frac{C_{of}}{C_b + C_{of}} \left(V_{Gf} - V_{FB}^f + \frac{C_b}{C_{of}}\psi_{sb} + \frac{Q_b}{2C_{of}} \right) \tag{6.10}$$

The transition between the strong inversion approximation regime and the depletion approximation regime occurs at $V = V_1$ which can be obtained from Eqs. (6.8) and (6.10). The result is

$$V_1 = \frac{C_{of}}{C_b + C_{of}} \left(V_{Gf} - V_{FB}^f + \frac{C_b}{C_{of}}\psi_{sb} + \frac{Q_b}{2C_{of}} \right) - 2\phi_B - ln(\beta Q_D^2/\lambda^2 C_{of}^2) \tag{6.11}$$

The front gate threshold voltage V_{Tf} is implied by the definition of V_1 [93]. In Eq. (6.11), V_{Gf} is equal to the V_{Tf} for which V_1 becomes equal to the source potential V_S, *i.e.*,

$$V_{Tf} = V_{FB}^f - \frac{C_b}{C_{of}}\psi_{sb} - \frac{Q_b}{2C_{of}} + \left(1 + \frac{C_b}{C_{of}}\right)\left[2\phi_B + V_S + \frac{1}{\beta} ln(\beta Q_D^2/\lambda^2 C_{of}^2)\right] \tag{6.12}$$

6.3 Current-Voltage Characteristics

For an n-channel SOI MOSFET, the drain current in the front channel is given by [93]

$$I_{Df} = -\frac{W}{L}\mu^*_{nf}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)} Q_{nf}\frac{dV}{d\psi_{sf}}d\psi_{sf} \tag{6.13}$$

where W is the channel width, L is the channel length, μ^*_{nf} is the effective mobility of front channel, Q_{nf} is given in Eq. (6.6), and $dV/d\psi_{sf}$ can be derived from Eqs. (6.3) and (6.6), which yield

$$\frac{dV}{d\psi_{sf}} = 1 + \frac{2}{\beta}\frac{\eta V_x + (\delta\lambda^2/2)\{1 - exp(-\beta\psi_{sb}) + exp[\beta(\psi_{sb} - 2\phi_B - V)]\} + \zeta\lambda^2/2}{V_x^2 - Q_D^2/C_{of}^2 + \zeta\lambda^2/\beta} \tag{6.14}$$

where $\delta = 1 - d\psi_{sb}/d\psi_{sf}$, $\eta = 1 + \delta(C_b/C_{of} + \lambda^2 C_{of}/2Q_D)$, $\zeta = exp(-\beta\psi_{sb}) - exp(-\beta\psi_{sf})$, and V_x is given in Eq. (6.9). For the MOSFET operating in depletion or inversion modes, the exponential terms in Eq. (6.14) are negligible [93], and Eq. (6.14) can be reduced to

$$\frac{dV}{d\psi_{sf}} = 1 + \frac{C_{of}[\delta\lambda^2 C_{of} - 2\eta(Q_{nf} + Q_D)]}{\beta Q_{nf}(Q_{nf} + 2Q_D)} \tag{6.15}$$

where Q_D and Q_{nf} are given in Eqs. (6.5) and (6.6), respectively. According to Eq. (6.15), one obtains

$$I_{Df} = -\frac{W}{L}\mu^*_{nf}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)}\left[Q_{nf} - (C_{of}/\beta)\left(\eta + \frac{\eta Q_{nf} - \delta\lambda^2 C_{of}}{Q_{nf} + 2Q_D}\right)\right]d\psi_{sf} \tag{6.16}$$

To reduce the complexity of Eq. (6.16), it is necessary to make the following assumption based on the charge-sheet model [93,94]

$$\frac{\eta Q_{nf} - \delta\lambda^2 C_{of}}{Q_{nf} + 2Q_D} \approx -\frac{\delta\lambda^2 C_{of}}{2Q_D} \tag{6.17}$$

which gives

$$I_{Df} = -\frac{W}{L}\mu^*_{nf}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)}[Q_{nf} - (C_{of}/\beta)(1 + \delta C_b/C_{of})]d\psi_{sf} \tag{6.18}$$

It is noted that a straight forward method (in Appendix 1) can be used to obtain the result of Eq. (6.18).

Two small signal parameters, drain conductance and transconductance, are derived from the current-voltage characteristics based on Eq. (6.13). The drain conductance, $g_d(= \partial I_{Df}/\partial V_D)$, can be expressed as

$$g_d = -\frac{W}{L}\mu_{nf}^* Q_{nf}|_{\psi_{sf}=\psi_{sf}(L)} \tag{6.19}$$

where Q_{nf} is given in Eq. (6.6) and $\psi_{sf}(L)$ can be obtained from Eqs. (6.3) and (6.6). The calculation of the transconductance, $g_m(= \partial I_{Df}/\partial V_{Gf})$ is more complex due to the dependence of $\psi_{sf}(0)$ and $\psi_{sf}(L)$ on V_{Gf} [93,95]. The general expression is

$$\begin{aligned} g_m = -\frac{W}{L}\mu_{nf}^* \Bigg\{ & \left[Q_{nf}\frac{dV}{d\psi_{sf}}\right]_{\psi_{sf}(L)} \frac{\partial\psi_{sf}(L)}{\partial V_{Gf}} - \left[Q_{nf}\frac{dV}{d\psi_{sf}}\right]_{\psi_{sf}(0)} \frac{\partial\psi_{sf}(0)}{\partial V_{Gf}} \\ & + \int_{\psi_{sf}(0)}^{\psi_{sf}(L)} \frac{\partial}{\partial V_{Gf}}\left(Q_{nf}\frac{dV}{d\psi_{sf}}\right) d\psi_{sf} \Bigg\} \end{aligned} \tag{6.20}$$

However, by considering $\psi_{sf}(0)$ and $\psi_{sf}(L)$ as independent of V_{Gf} [94], a good approximation can be obtained as

$$g_m = \frac{W}{L}\mu_{nf}^* C_{of}[\psi_{sf}(L) - \psi_{sf}(0)] \tag{6.21}$$

where $\psi_{sf}(0)$ and $\psi_{sf}(L)$ can be evaluated by Eqs. (6.3) and (6.6). The same expressions of the bulk counterpart for Eqs. (6.19) and (6.21) have been derived in Van de Wiele [93].

The relationship between ψ_{sf} and ψ_{sb} has to be established for the numerical resolution of the equations in the previous discussion. This can be achieved by specifying the condition of the back gate. Two cases will be demonstrated:

6.3.1 Back Surface Depleted from Source to Drain

When the back surface is depleted, the back surface carrier charge density $Q_{cb} = 0$, and the back surface potential is given by [86]

$$\psi_{sb} = \frac{C_{ob}}{C_{ob} + C_b}\left[V_{Gb} - V_{FB}^b + \frac{C_b}{C_{ob}}\psi_{sf} + \frac{Q_b}{2C_{ob}}\right], \tag{6.22}$$

$$\delta = \frac{C_{ob}}{C_{ob} + C_b}, \tag{6.23}$$

$$\eta = 1 + \frac{C_{bb}}{C_{of}} + \frac{\lambda^2 C_{of} C_{ob}}{2(C_{ob} + C_b)Q'_D}, \tag{6.24}$$

and from Eq. (6.6)

$$Q_{nf} = -C_{of}\left[V_{Gf} - V_{FB}^f - \left(1 + \frac{C_{bb}}{C_{of}}\right)\psi_{sf} + \left(\frac{C_{bb}}{C_{of}}\right)(V_{Gb} - V_{FB}^b) + \frac{(2C_b + C_{ob})Q_b}{2C_{of}(C_b + C_{ob})}\right] \tag{6.25}$$

where $C_{bb} = C_b C_{ob}/(C_b + C_{ob})$, and

$$Q'_D = -\lambda C_{of}\left[\frac{C_{ob}}{C_b + C_{ob}}\left(\psi_{sf} - V_{Gb} + V_{FB}^b - \frac{Q_b}{2C_{ob}}\right)\right]^{1/2} \tag{6.26}$$

In Eq. (6.22), the fast surface states at the back Si/SiO$_2$ interface is neglected for simplicity and all symbols have their usual meanings. According to Eq. (6.22) and the general assumption $\psi_{sf}(0) \approx 2\phi_B + V_S$ for a strongly inverted front surface, the front-gate threshold voltage in Eq. (6.12) can be expressed as

$$V_{Tf}^{(2)} = V_{Tf}^{(1)} + \left(1 + \frac{C_{bb}}{C_{of}}\right)V_S + \frac{1}{\beta}\left(1 + \frac{C_b}{C_{of}}\right)ln(\beta Q_x^2/\lambda^2 C_{of}^2) \tag{6.27}$$

where

$$V_{Tf}^{(1)} = V_{FB}^f + \left(1 + \frac{C_{bb}}{C_{of}}\right)2\phi_B - \left(\frac{C_{bb}}{C_{of}}\right)(V_{Gb} - V_{FB}^b) - \frac{(2C_b + C_{ob})Q_b}{2C_{of}(C_b + C_{ob})}, \tag{6.28}$$

and

$$Q_x = -\lambda C_{of}\left[\frac{C_{ob}}{C_b + C_{ob}}\left(2\phi_B + V_S - V_{Gb} + V_{FB}^b - \frac{Q_b}{2C_{ob}}\right)\right]^{1/2} \tag{6.29}$$

The general drain current can be obtained from Eqs. (6.16) and (6.25) as

$$I_{Df} = I_{Df}^{(3)} + \Delta I_{Df}^D \tag{6.30}$$

where

$$\begin{aligned} I_{Df}^{(3)} &= \frac{W}{L}\mu_{nf}^* C_{of}\left\{\left[V_y + \frac{1}{\beta}\left(1 + \frac{C_{bb}}{C_{of}}\right)\right][\psi_{sf}(L) - \psi_{sf}(0)]\right. \\ &\left.\quad -\frac{1}{2}\left(1 + \frac{C_{bb}}{C_{of}}\right)[\psi_{sf}^2(L) - \psi_{sf}^2(0)]\right\} \end{aligned} \tag{6.31}$$

and

$$V_y = V_{Gf} - V_{FB}^f + \left(\frac{C_{bb}}{C_{of}}\right)(V_{Gb} - V_{FB}^b) + \frac{(2C_b + C_{ob})Q_b}{2C_{of}(C_b + C_{ob})} \tag{6.32}$$

is obtained from the charge-sheet model in Eq. (6.18), and ΔI_{Df}^D (in Appendix 2) accounts for the difference of the present model from the charge-sheet model. If the assumptions $\psi_{sf}(0) \approx 2\phi_B + V_S$ and $\psi_{sf}(L) \approx 2\phi_B + V_D$ are employed in Eq. (6.31) for strong inversion, then Eq. (6.31) can be reduced to

$$I_{Df}^{(2)} = I_{Df}^{(1)} + \frac{W}{L}\mu_{nf}^* C_{of}\beta^{-1}(1 + C_{bb}/C_{of})V_{DS} \tag{6.33}$$

where

$$I_{Df}^{(1)} = \frac{W}{L}\mu_{nf}^* C_{of}\left[(V_{Gf} - V_{Tf}^{(1)})V_{DS} - \frac{(1 + C_{bb}/C_{of})(V_D^2 - V_S^2)}{2}\right] \tag{6.34}$$

It is noted that Eqs. (6.28) and (6.34) are the same as those derived in [77] and [86], respectively, and they are only the first order approximations.

6.3.2 Back Surface Accumulated from Source to Drain

When the back surface is accumulated, the back surface potential is virtually pinned at zero [77], *i.e.*,

$$\psi_{sb} \approx 0, \tag{6.35}$$

$$\delta = 1, \tag{6.36}$$

$$\eta = 1 + \frac{C_b}{C_{of}} - \frac{\lambda}{2}(\psi_{sf})^{-1/2} \tag{6.37}$$

and

$$Q_{nf} = -C_{of}\left[V_{Gf} - V_{FB}^f - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf} + \frac{Q_b}{2C_{of}}\right] \tag{6.38}$$

From Eqs. (6.12), (6.35), and the assumption $\psi_{sf}(0) \approx 2\phi_B + V_S$, the front gate threshold voltage can be obtained as

$$V_{Tf}'' = V_{Tf}' + \left(1 + \frac{C_b}{C_{of}}\right)\left[V_S + \frac{1}{\beta}ln(\beta Q_y^2/\lambda^2 C_{of}^2)\right] \tag{6.39}$$

where

$$Q_y = -\lambda C_{of}(2\phi_B + V_S)^{1/2}, \tag{6.40}$$

and

$$V'_{Tf} = V^f_{FB} + \left(1 + \frac{C_b}{C_{of}}\right) 2\phi_B - \frac{Q_b}{2C_{of}} \tag{6.41}$$

is the first order approximation of Eq. (6.12) for accumulated back surface. The same expression for Eq. (6.41) bas been reported in Lim and Fossum [77]. The drain current for the back surface accumulation can be expressed from Eqs. (6.16) and (6.38) as

$$I_{Df} = I'''_{Df} + \Delta I^A_{Df} \tag{6.42}$$

where

$$\begin{aligned} I'''_{Df} &= \frac{W}{L}\mu^*_{nf}C_{of}\left\{\left[V_z + \frac{1}{\beta}\left(1 + \frac{C_b}{C_{of}}\right)\right][\psi_{sf}(L) - \psi_{sf}(0)]\right. \\ &\left. -\frac{1}{2}\left(1 + \frac{C_b}{C_{of}}\right)[\psi^2_{sf}(L) - \psi^2_{sf}(0)]\right\} \end{aligned} \tag{6.43}$$

and

$$V_z = V_{Gf} - V^f_{FB} + \frac{Q_b}{2C_{of}} \tag{6.44}$$

is approximated by the charge-sheet model in Eq. (6.18). ΔI^A_{Df} (in Appendix 2) is the current deviation of the present model from the charge-sheet model. From the assumptions $\psi_{sf}(0) \approx 2\phi_B + V_S$ and $\psi_{sf}(L) \approx 2\phi_B + V_D$, Eq. (6.43) can be reduced to

$$I''_{Df} = I'_{Df} + \frac{W}{L}\mu^*_{nf}C_{of}\beta^{-1}(1 + C_b/C_{of})V_{DS} \tag{6.45}$$

where

$$I'_{Df} = \frac{W}{L}\mu^*_{nf}C_{of}\left[(V_{Gf} - V'_{Tf})V_{DS} - \frac{(1 + C_b/C_{of})(V^2_D - V^2_S)}{2}\right] \tag{6.46}$$

is the first order approximation of the drain current for an accumulated back surface, as indicated in Lim and Fossum [86].

6.4 Results and Discussion

A typical SOI MOSFET with $t_{of} = 200$ Å, $t_{ob} = 0.4\ \mu m$, $t_f = 0.2\ \mu m$, $W/L = 2$, and $N_A = 1 \times 10^{16}$ cm^{-3} under the assumptions $V_{FB}^f = V_{FB}^b = 0$, $V_S = 0$, and the body potential $V_B = 0$ for accumulated back surface is considered to evaluate the quantities derived in this model.

The back gate surface is shown to be depleted for V_{Gb}=0 V and accumulated for V_{Gb}=−20 V for the given device [77]. By numerical resolution of Eqs. (6.3) and (6.6), the relationship between the front surface potential ψ_{sf} and the potential $V(y)$ for different front-gate potentials and back-gate bias conditions are shown in Fig. 6.2. The two- (strongly and weakly inverted) region approximation fits well as indicated in the figure. The intersection of these two regions gives the potential V_1 in Eq. (6.11) which in turn defines the threshold voltage. Figure 6.3 illustrates the dependence of V_{Tf} on V_{Gb} for various film thicknesses. As illustrated in the present model [Eqs. (6.27) and (6.39)], V_{Tf} is approximately propotional to t_b^{-1} for accumulated back surface and is almost independent of t_b for depleted back surface. The intersection of Eqs. (6.27) and (6.39) gives the back-gate potential V_{Gb}^A which is the maximum bias needed to make the back surface accumulated. It is also noted from Fig. 6.3 that the discrepancy of V_{Tf} between this model and the model in Lim and Fossum [77] [Eqs. (6.28) and (6.41)] increases as the film thickness decreases. However, for depleted back surface, which is a better mode of operation [96], the discrepancy is small at back gate bias around zero.

The important feature of the current-voltage characteristics developed in this model [Eq. (6.16)] is that it is valid in all regions of operation of the SOI MOSFET and no particular assumption must be introduced for the saturation regime. Figures 6.4 and 6.5 show the drain currents from different models for depleted and accumulated back surface, respectively. For comparison, the drain current (calculated from Eq. (36) [90]) of the bulk counterpart with the same parameters is also shown in both figures. In Fig. 6.5, the floating-body bipolar effects [97] which account for the body potential is neglected for simplicity, and an effective mobility μ^*_{nf}=450 cm$^2/V \cdot sec$ is used in the calculation of these curves in both figures. In fact, mobility varies along the channel and is a function of the normal and lateral electric fields [88,93]. It is noted that the saturated drain current (occurs at $V_D > V_{D(sat)}$) in Fig. 6.5 for accumulated back surface is smaller than that for depleted back surface in Fig. 6.4. This phenomenon is explained by the higher threshold voltage for accumulated back surface as shown in Fig. 6.3. The drain voltage $V_{D(sat)}$ for calculating the saturated drain current of Eqs. (6.34) and (6.46) can be obtained [86] as

$$V^{(1)}_{D(sat)} = \frac{V_{Gf} - V^{(1)}_{Tf}}{1 + C_{bb}/C_{of}} \tag{6.47}$$

for depleted back surface and

$$V'_{D(sat)} = \frac{V_{Gf} - V'_{Tf}}{1 + C_b/C_{of}} \tag{6.48}$$

for accumulated back surface. In both figures, the drain currents from the charge-sheet model [Eqs. (6.31) and (6.43)] seem very close to the present model [Eqs. (6.30) and (6.42)]. However, the strong-inversion assumption [Eqs. (6.34) and (6.46)] deviates from the model by a significant amount for present cases. The percentage error with respect to the proposed model for different models is plotted as a function of the front gate bias in Fig. 6.6. The error is evaluated for saturated drain current. From the figure, it is apparent that the charge-sheet model possesses less than 6% error over the entire gate bias range and less than 2% for $V_{Tf} \geq 3$ V. Although the strong-inversion assumption shows an error larger than 10% for $V_{Gf} \leq 5$ V in this case, it may be considered a good approximation for $V_{Gf} > 5$ V. It should be noted that the error is strongly dependent on the parameters of devices.

Figures 6.7 and 6.8 show the conductances obtained from the proposed model [Eq. (6.19)] and the strong-inversion assumption as a function of the drain voltage. In this simulation, the effects of source and drain resistances are neglected. The conductance for the strong-inversion assumption can be derived from Eqs. (6.34) or

(6.46) by [86]

$$g_d^{(1)} = \frac{W}{L}\mu_{nf}^{*}C_{of}[V_{Gf} - V_{Tf}^{(1)} - (1 + C_{bb}/C_{of})V_{DS}] \tag{6.49}$$

for depleted back surface and

$$g_d^{'} = \frac{W}{L}\mu_{nf}^{*}C_{of}[V_{Gf} - V_{Tf}^{'} - (1 + C_{b}/C_{of})V_{DS}] \tag{6.50}$$

for accumulated back surface. The difference of the conductance between these two models decreases as the drain potential increases, and is larger for higher front gate voltage. The asymptotic behavior of the transconductance [Eq. (6.21)] as a function of the front gate voltage, which is related to the asymptotic behavior of $\psi_{sf}(0)$ and $\psi_{sf}(L)$, is plotted in Fig. 6.9. The transconductance in the linear regime for the strong-inversion assumption can be deduced from Eqs. (6.34) or (6.46) as [86]

$$g_m^{(1)} = \frac{W}{L}\mu_{nf}^{*}C_{of}V_{DS} \tag{6.51}$$

which is independent of V_{Gf} if the mobility degradation is neglected for high V_{Gf}. In the saturation regime, V_{DS} in Eq. (6.51) is replaced by $V_{D(sat)}^{(1)}$ in Eq. (6.47) for back surface depletion and $V_{D(sat)}^{'}$ in Eq. (6.48) for back surface accumulation. The transconductance varies linearly with V_{Gf} in the saturation regime. From Figs. 6.4, 6.5, and 6.7-9, it is apparent that in the respects of drain current, conductance, and transconductance, a fully depleted SOI MOSFET operated in depleted back surface mode is superior to the bulk counterpart, although this is not true for one operated in accumulated back surface mode.

Figure 6.10 shows the measured and calculated current-voltage characteristics of a representative device with W=2.4 μm, L=3.6 μm, t_f ≈1700 Å, t_{of}=150 Å, t_{ob} ≈3300 Å, and N_A ≈3.5×10^{16} cm^{-3} for V_S=0 V. The body potential was selected to zero for accumulated back surface. For the calculation of I_{Df}, the threshold voltages [$V_{Tf}^{D}(V_{Gb} = 0V)$ ≈0.45 V, $V_{Tf}^{A}(V_{Gb} = -40V)$ ≈0.5 V] and effective electron mobility (μ_{nf}^{*} ≈480 cm^2/V·sec) were determined from the measured $I_{Df}(V_{Gf})$ in the linear region. Good agreement was observed between the measured and calculated results.

The slight discrepancy at V_{Gf}=2 V and high V_{DS} can be explained by the dependences of μ_{nf}^{*} on the terminal voltages and short-channel effects [86,88].

6.5 Conclusion

A fully depleted SOI MOSFET model valid for long-channel devices has been developed. This model analytically describes the drain current, conductance, and transconductance for all regions of operation. The model accounts for the charge coupling between the front and the back gates, and eliminates the complicated integrals needed for the inversion charge density and drain current. In this model, the charge-sheet model and strong-inversion assumption are contained as approximations. The fact that the charge-sheet model is accurate to within 6% implies that it is a good approximation for long-channel SOI MOSFETs.

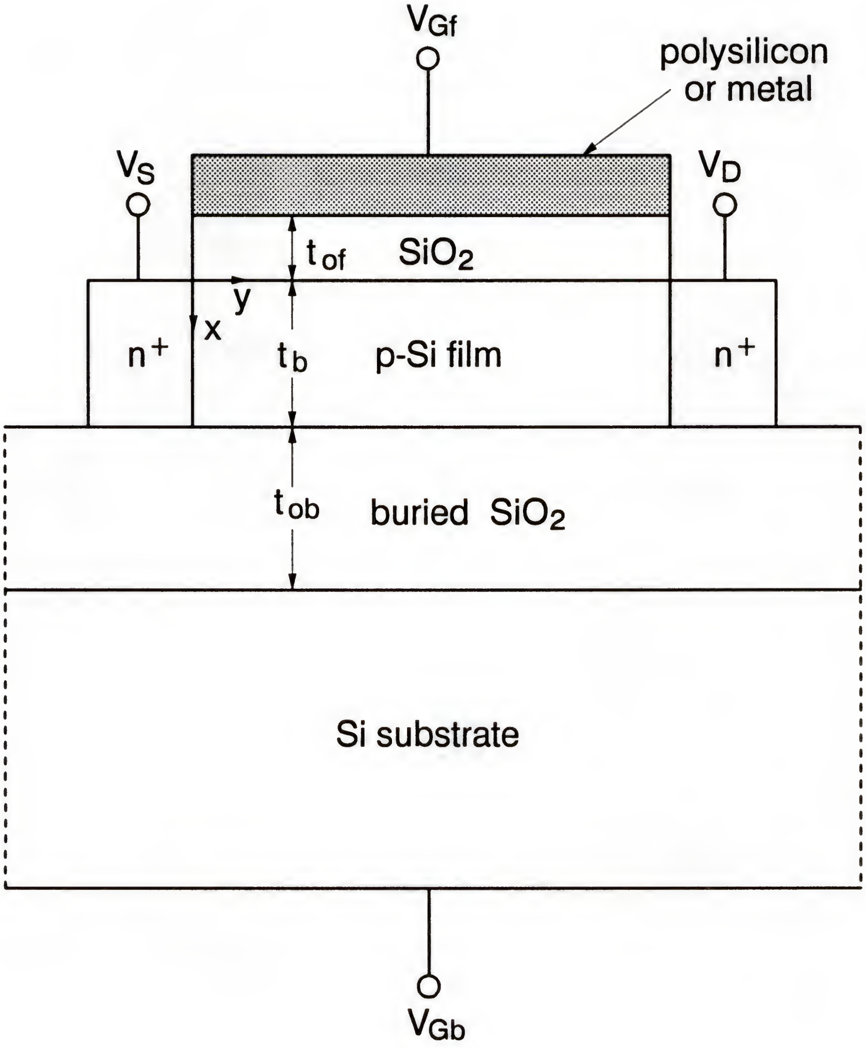


Figure 6.1 An n-channel SOI MOSFET structure.

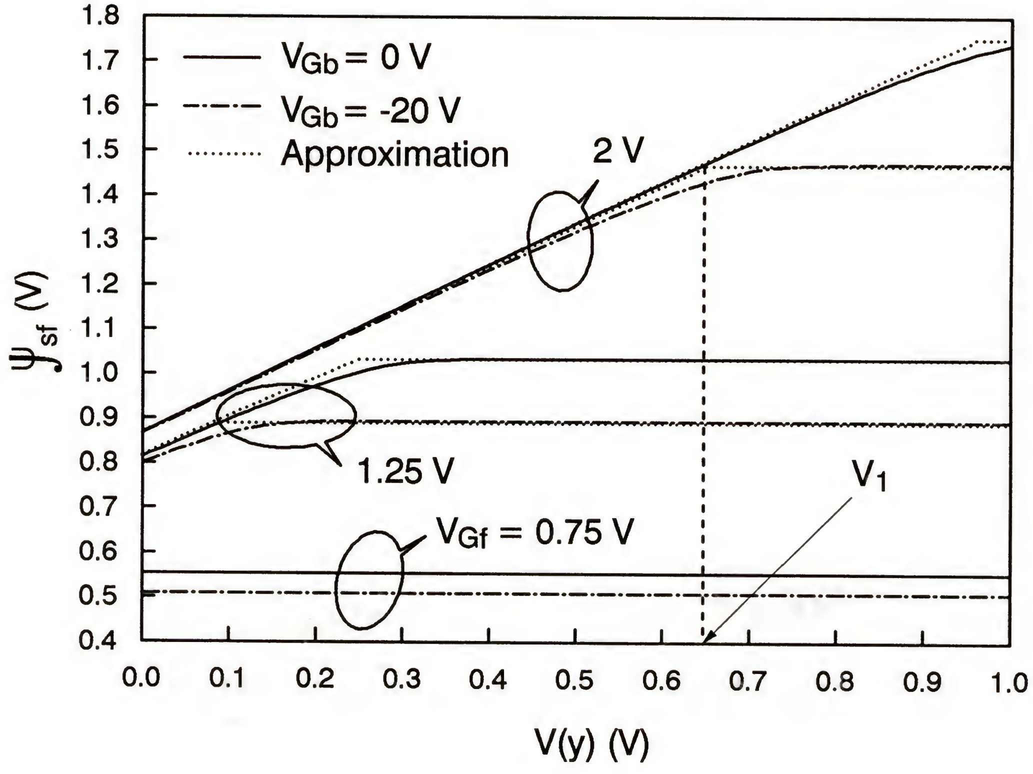


Figure 6.2 Front surface potential ψ_{sf} versus channel potential V for different front-gate potentials and back-gate bias. The approximation is obtained from Eqs. (6.8) and (6.10).

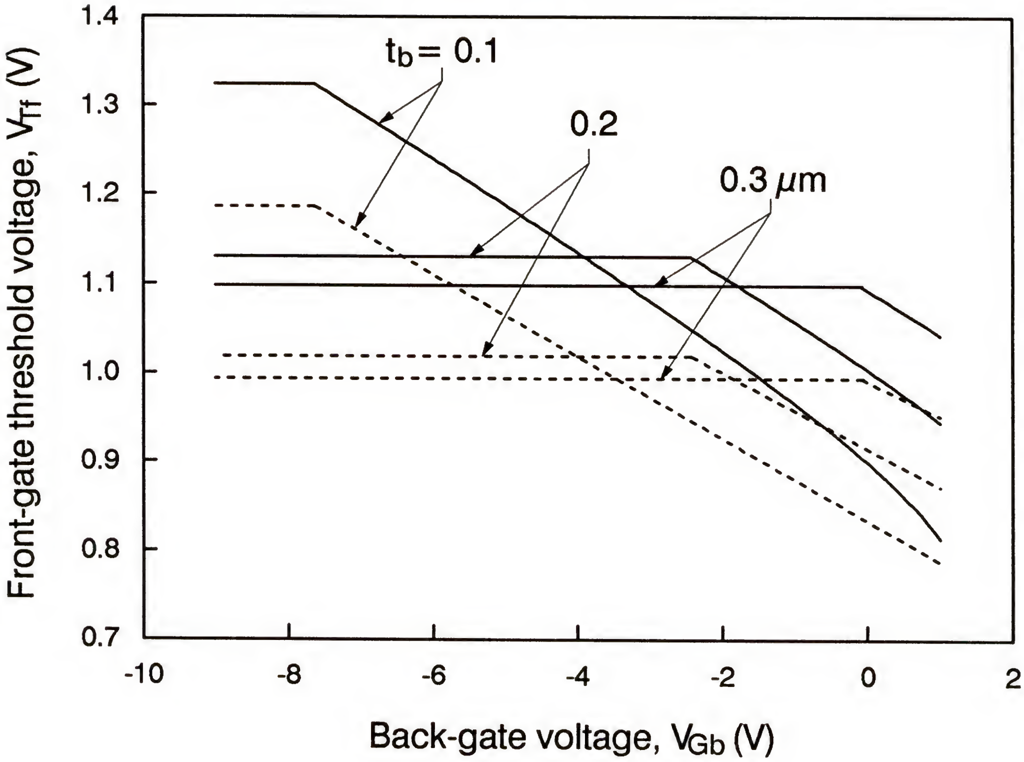


Figure 6.3 Theoretical dependence of V_{Tf} on V_{Gb} for fully-depleted SOI MOSFETs with various thicknesses. The solid lines are obtained from Eqs. (6.27) and (6.39), and dash lines are from Eqs. (6.28) and (6.41).

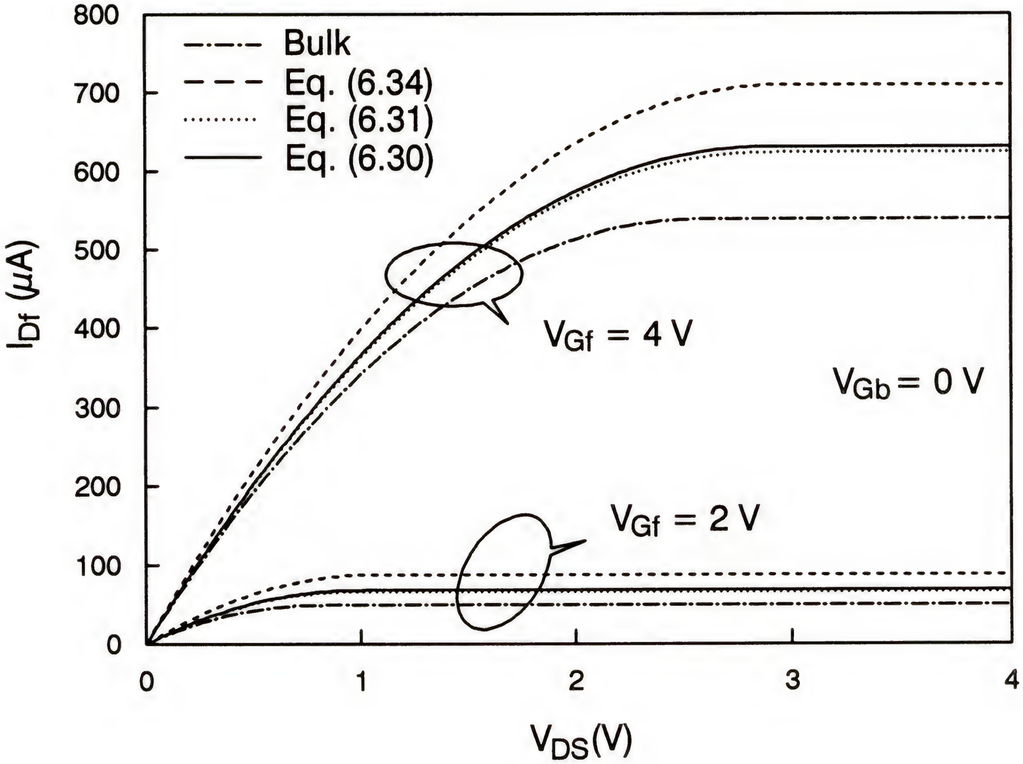


Figure 6.4 Drain current-voltage characteristics of the SOI MOSFET and bulk counterpart for depleted back surface (V_{Gb}=0 V) evaluated from the present model [Eq. (6.30)], charge-sheet model [Eq. (6.31)], and strong-inversion approximation [Eq. (6.34)].

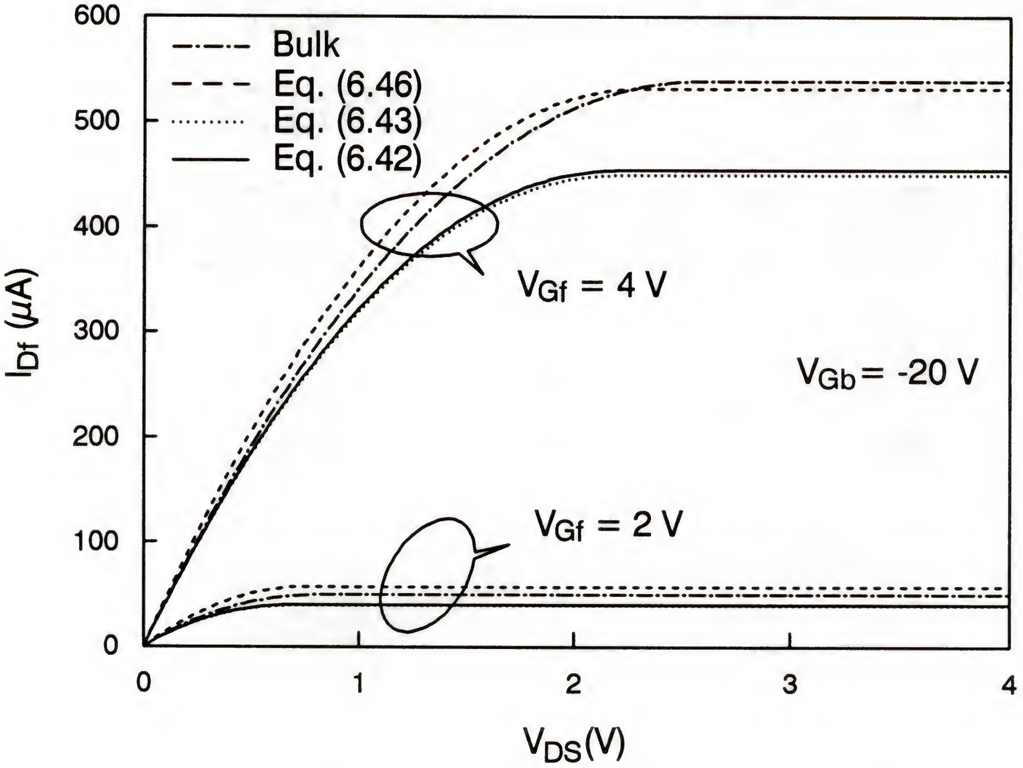


Figure 6.5 Drain current-voltage characteristics of the SOI MOSFET and bulk counterpart for accumulated back surface (V_{Gb}=−20 V) evaluated from the present model [Eq. (6.42)], charge-sheet model [Eq. (6.43)], and strong-inversion approximation [Eq. (6.46)].

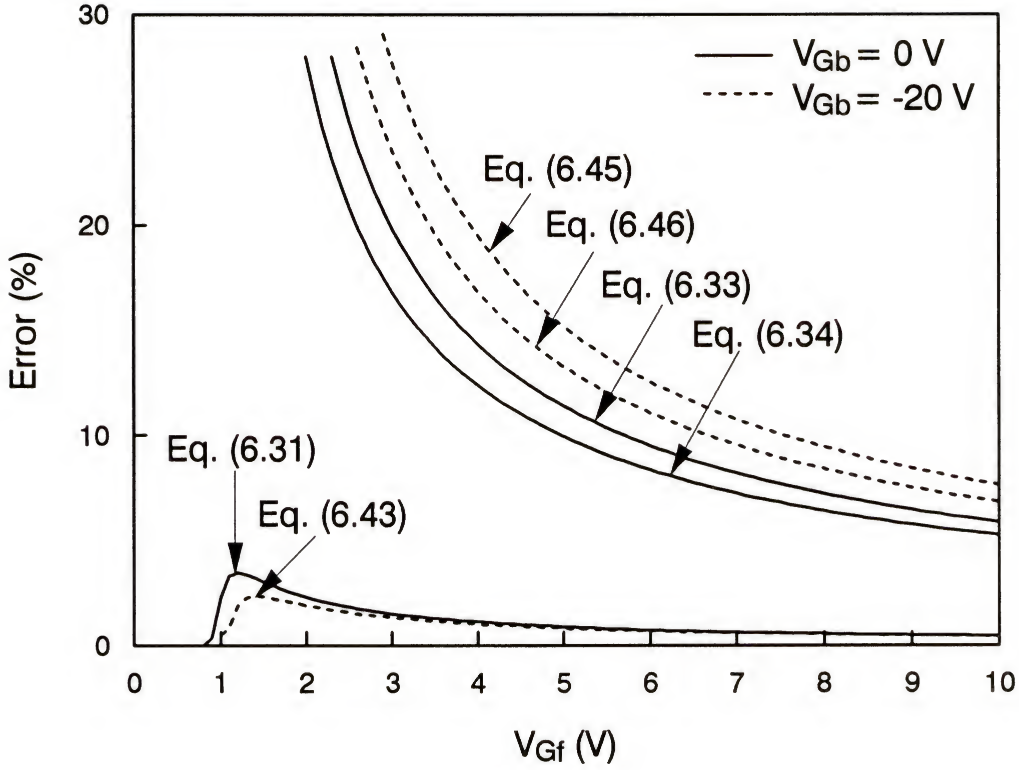


Figure 6.6 Percentage of drain current error in the saturation region with respect to the proposed model [Eq. (6.30) for V_{Gb}=0 V and Eq. (6.42) for $V_{Gb}=-20$ V] for the strong-inversion approximation [Eqs. (6.34) and (6.46)] and charge-sheet model [Eqs. (6.31) and (6.43)].

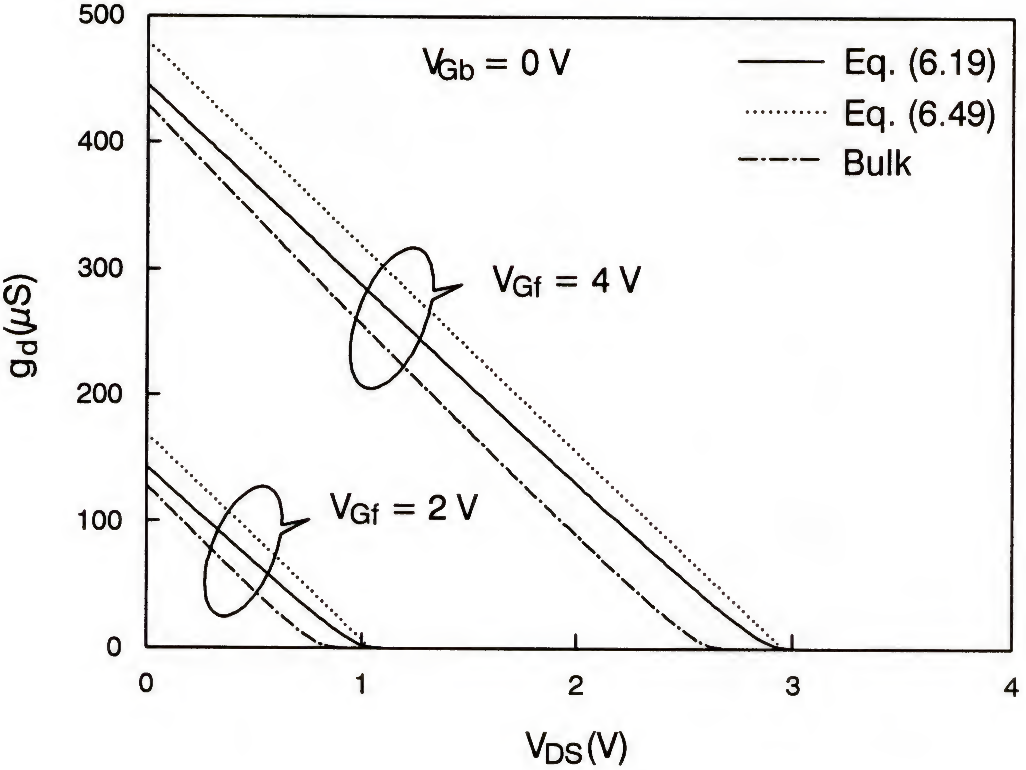


Figure 6.7 Drain conductance versus voltage V_{DS} of the SOI MOSFET and bulk counterpart for various front-gate potentials and depleted back surface: the proposed model [Eq. (6.19)] and strong-inversion approximation [Eq. (6.49)].

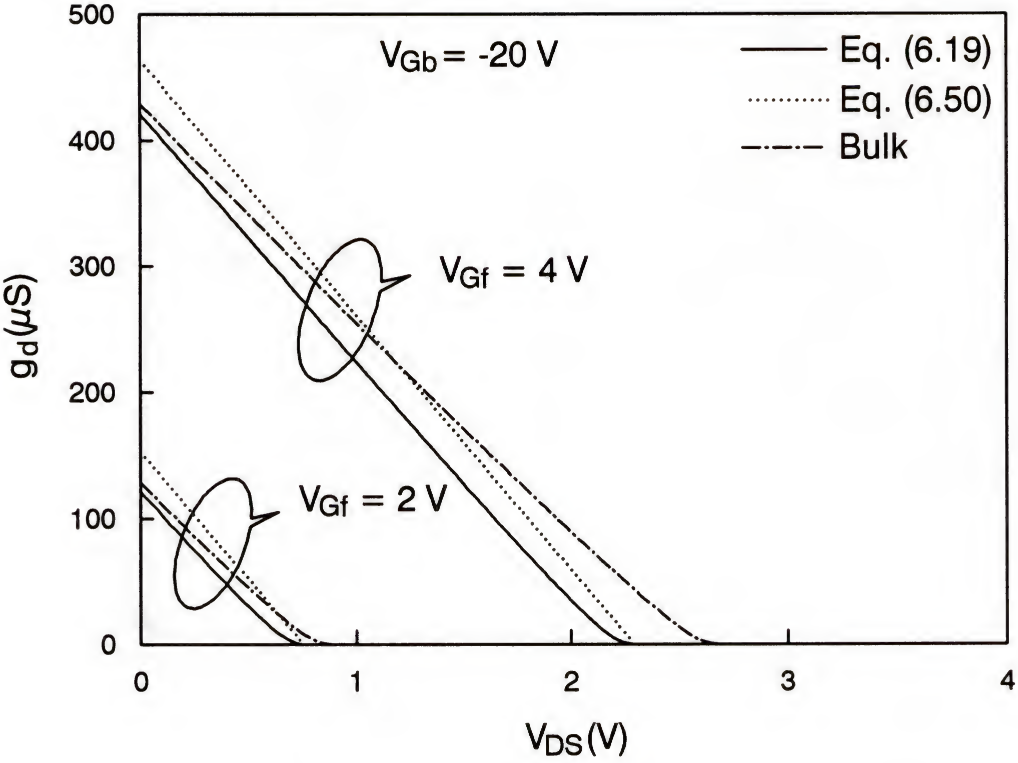


Figure 6.8 Drain conductance versus voltage V_{DS} of the SOI MOSFET and bulk counterpart for various front-gate potentials and accumulated back surface: the proposed model [Eq. (6.19)] and strong-inversion approximation [Eq. (6.50)].

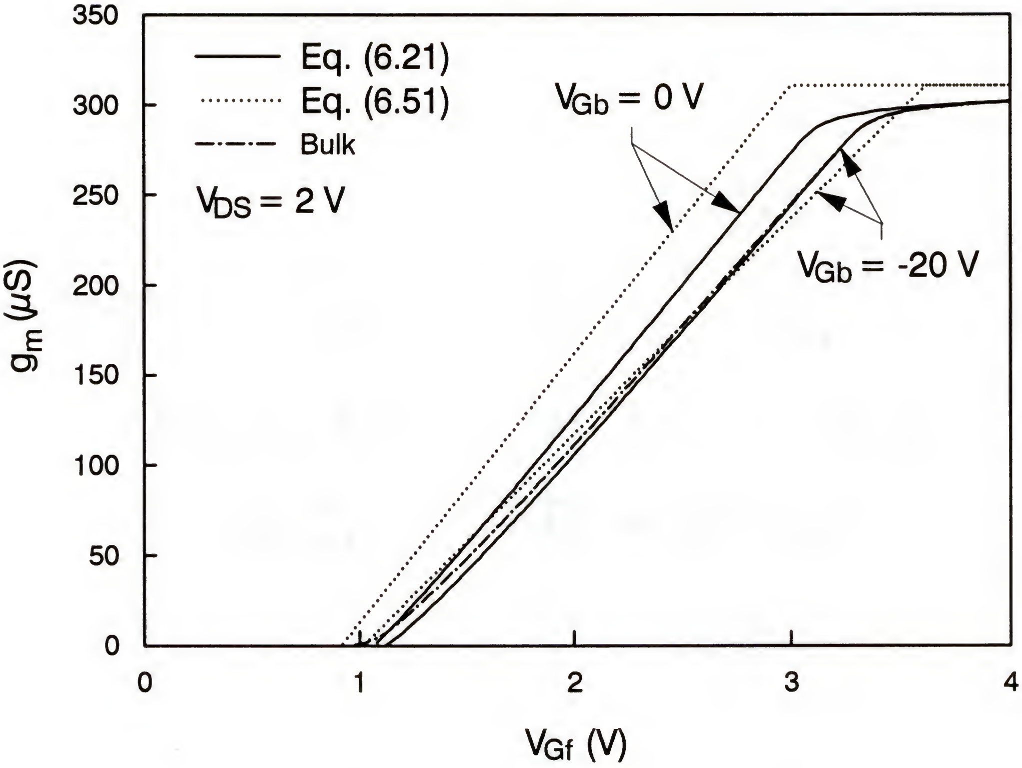


Figure 6.9 Transconductance versus front-gate voltage of the SOI MOSFET and bulk counterpart at V_{DS}=2 V for the present model [Eq. (6.21)] and strong-inversion approximation [Eq. (6.51)].

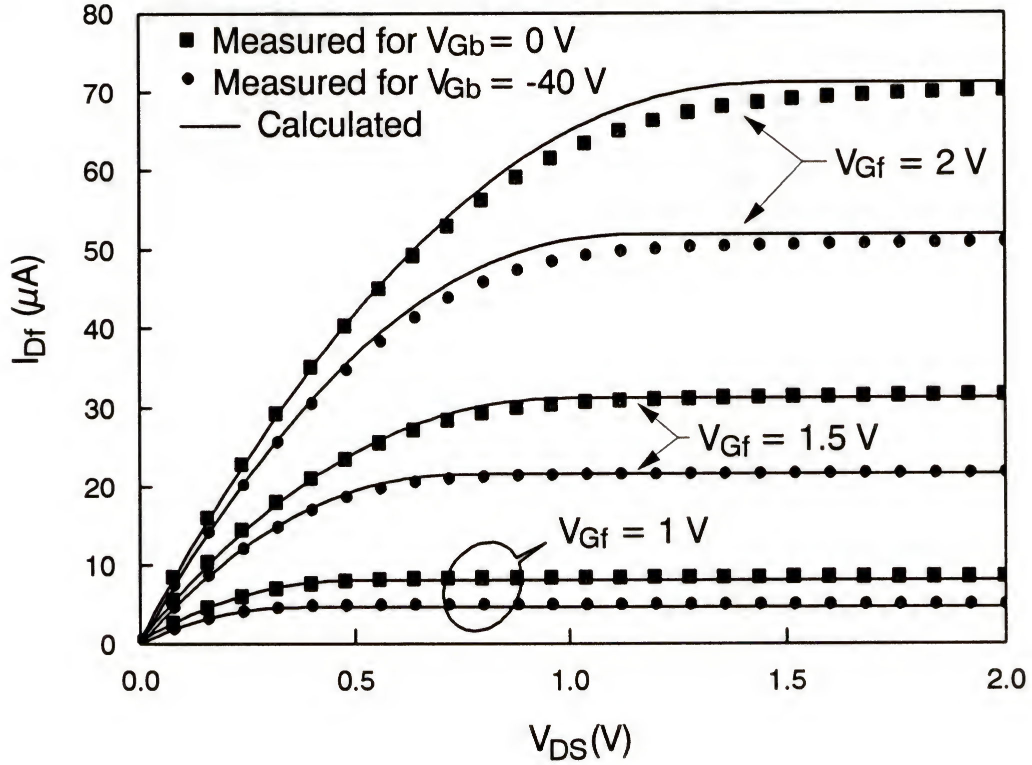


Figure 6.10 Measured and calculated [Eqs. (6.30) and (6.42)] current-voltage characteristics of the SOI MOSFET described in the last paragraph of Section 6.4.

CHAPTER 7
NUMERICAL ANALYSIS OF SMALL-SIGNAL CHARACTERISTICS OF A FULLY DEPLETED SOI MOSFET

7.1 Introduction

Devices fabricated on thin film silicon-on-insulator (SOI) technology has recently received much attention due to the advantages of improved isolation and design flexibility as compared to that fabricated by bulk technology. The characteristics of fully depleted SOI MOSFETs differ from the bulk counterparts due to effects of the thin body and the charge coupling between the front and back gates. Several models that account for the structural uniqueness of the device have been reported [86-89] recently. For analog SOI MOSFET circuit design, it is essential to have the detailed knowledge of small-signal characteristics in the devices. An accurate small-signal model is necessary for the prediction and optimization of device performance. A simple model [87] reported recently is only valid in strong inversion and presents discontinuities for the model parameters transit from cutoff to triode region.

In this chapter, we modify the existing bulk MOSFET small-signal model [95] for the fully depleted SOI counterpart by emphasizing the structural uniqueness of the devices. Under quasistatic operation, the model parameters valid for all regions of operation, including weak and moderate inversion, are derived and computed by using the theories proposed in Chapter 6. The numerical results of model parameters for both depleted and accumulated back surface are presented. The results show no discontinuities in the capacitance-voltage characteristics compared with that from the strong-inversion theory. For simplicity, higher order effects such as effective mobility variation and short channel effects [88] are ignored.

7.2 Expressions of Small-Signal Parameters

For a fully depleted SOI MOSFET, the charge coupling between the front and back gate becomes important if the buried oxide is thin enough, and consequently the performance of the device depends on the back-gate bias as well as the properties of the front surface (front-gate-oxide/Si-film interface). When the back surface is depleted and the body floating, the back surface potential ψ_{sb} is not an explicit function of body potential V_B [86], and the small-signal equivalent circuit of the SOI MOSFET is given in Fig. 7.1. This equivalent circuit is similar to the bulk MOSFET [95] except that the body terminal is replaced by the back-gate. For back surface accumulation, ψ_{sb} is approximately equal to V_B (which is near zero for quasistatic operation) and is independent of back-gate voltage V_{Gb} [87]. Figure 7.2 shows the small-signal equivalent circuit for accumulated back surface. The intrinsic capacitors in the equivalent circuits of Figs. 7.1 and 7.2 can be expressed as

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j} \tag{7.1}$$

where i, j=Gf, Gb, D, S, and B denote front-gate, back-gate, drain, source, and body, respectively. The front-gate charge Q_{Gf}, back-gate charge Q_{Gb}, body charge Q_B, source charge Q_S, and drain charge Q_D are defined as follows [87,95]:

$$Q_{Gf} = -\frac{W^2\mu_{nf}^*}{I_{Df}}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)} Q_{gf}Q_{nf}\frac{dV}{d\psi_{sf}}d\psi_{sf}, \tag{7.2}$$

$$Q_{Gb} = -\frac{W^2\mu_{nf}^*}{I_{Df}}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)} Q_{gb}Q_{nf}\frac{dV}{d\psi_{sf}}d\psi_{sf}, \tag{7.3}$$

$$Q_B = -\frac{W^2\mu_{nf}^*}{I_{Df}}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)} (Q_{nb}+Q_b)Q_{nf}\frac{dV}{d\psi_{sf}}d\psi_{sf}, \tag{7.4}$$

$$Q_S = -\frac{W^2\mu_{nf}^*}{I_{Df}}\int_{\psi_{sf}(0)}^{\psi_{sf}(L)} \left(1-\frac{I_{Df}(\psi_{sf})}{I_{Df}}\right) Q_{nf}^2\frac{dV}{d\psi_{sf}}d\psi_{sf}, \tag{7.5}$$

and

$$Q_D = -\frac{W^2\mu_{nf}^*}{I_{Df}} \int_{\psi_{sf}(0)}^{\psi_{sf}(L)} \frac{I_{Df}(\psi_{sf})}{I_{Df}} Q_{nf}^2 \frac{dV}{d\psi_{sf}} d\psi_{sf} \tag{7.6}$$

where W is the channel width, L is the channel length, μ_{nf}^* is the effective electron mobility of front channel, and ψ_{sf} is the front surface potential. The front-gate charge density Q_{gf}, back-gate charge density Q_{gb}, depletion-region charge density Q_b, inversion (electron) charge density of the front channel Q_{nf}, and inversion (electron) charge density of the back channel Q_{nb} are given by [77,87]

$$Q_{gf} = C_{of}(V_{Gf} - V_{FB}^f - \psi_{sf}), \tag{7.7}$$

$$Q_{gb} = C_{ob}(V_{Gb} - V_{FB}^b - \psi_{sb}), \tag{7.8}$$

$$Q_b = -qN_A t_b, \tag{7.9}$$

$$Q_{nf} = -C_{of}\left[V_{Gf} - V_{FB}^f - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf} + \frac{C_b}{C_{of}}\psi_{sb} + \frac{Q_b}{2C_{of}}\right], \tag{7.10}$$

and

$$Q_{nb} = -C_{ob}\left[V_{Gb} - V_{FB}^b + \frac{C_b}{C_{ob}}\psi_{sf} - \left(1 + \frac{C_b}{C_{ob}}\right)\psi_{sb} + \frac{Q_b}{2C_{ob}}\right] \tag{7.11}$$

The symbols in Eqs. (7.7)-(7.11) have their usual meaning. For depleted back surface, the drain current $I_{Df} = I_{Df}^D$ is given in Chapter 6 by

$$\begin{aligned} I_{Df}^D &= \frac{W}{L}\mu_{nf}^* C_{of}\left\{\left[V_y + \frac{1}{\beta}\left(1 + \frac{C_{bb}}{C_{of}}\right)\right][\psi_{sf}(L) - \psi_{sf}(0)]\right. \\ &\left. -\frac{1}{2}\left(1 + \frac{C_{bb}}{C_{of}}\right)[\psi_{sf}^2(L) - \psi_{sf}^2(0)]\right\} + \Delta I_{Df}^D \end{aligned} \tag{7.12}$$

where $C_{bb} = C_b C_{ob}/(C_b + C_{ob})$, $V_y = V_{Gf} - V_{FB}^f + C_{bb}(V_{Gb} - V_{FB}^b)/C_{of} + (2C_b + C_{ob})Q_b/2C_{of}(C_b + C_{ob})$, and ΔI_{Df}^D is given by Eq. (B.1) in Appendix 2. For accumulated back surface, $I_{Df} = I_{Df}^A$ is given in Chapter 6 by

$$\begin{aligned} I_{Df}^A &= \frac{W}{L}\mu_{nf}^* C_{of}\left\{\left[V_z + \frac{1}{\beta}\left(1 + \frac{C_b}{C_{of}}\right)\right][\psi_{sf}(L) - \psi_{sf}(0)]\right. \\ &\left. -\frac{1}{2}\left(1 + \frac{C_b}{C_{of}}\right)[\psi_{sf}^2(L) - \psi_{sf}^2(0)]\right\} + \Delta I_{Df}^A \end{aligned} \tag{7.13}$$

where $V_z = V_{Gf} - V_{FB}^f + Q_b/2C_{of} + C_bV_B/C_{of}$, and

$$\Delta I_{Df}^A = \frac{W}{L}\mu_{nf}^*C_{of}\frac{1}{\beta}\left\{\left(1+\frac{C_b}{C_{of}}\right)[\psi_{sf}(L)-\psi_{sf}(0)]\right.$$

$$+2\lambda\{[\psi_{sf}(L)-V_B]^{1/2}-[\psi_{sf}(0)-V_B]^{1/2}\}$$

$$+\frac{2\lambda C_{of}}{K}\left(V_{z1}+\frac{\lambda^2C_{of}}{C_{of}+C_b}\right)ln\left[\frac{\{[\psi_{sf}(L)-V_B]^{1/2}-s_3\}\{[\psi_{sf}(0)-V_B]^{1/2}-s_4\}}{\{[\psi_{sf}(L)-V_B]^{1/2}-s_4\}\{[\psi_{sf}(0)-V_B]^{1/2}-s_3\}}\right]$$

$$\left.+\frac{2\lambda^2C_{of}}{C_{of}+C_b}ln\left[\frac{\{[\psi_{sf}(L)-V_B]^{1/2}-s_3\}\{[\psi_{sf}(L)-V_B]^{1/2}-s_4\}}{\{[\psi_{sf}(0)-V_B]^{1/2}-s_3\}\{[\psi_{sf}(0)-V_B]^{1/2}-s_4\}}\right]\right\} \tag{7.14}$$

here $K = [\lambda^2C_{of}^2 + V_{z1}C_{of}(C_{of}+C_b)]^{1/2}$, $s_3 = (\lambda C_{of}+K)/(C_{of}+C_b)$, $s_4 = (\lambda C_{of} - K)/(C_{of}+C_b)$, and $V_{z1} = V_z - (C_b + C_{of})V_B/C_{of}$.

The front-gate transconductance g_m and drain conductance g_d are given in Chapter 6 by

$$g_d = -\frac{W}{L}\mu_{nf}^*Q_{nf}|_{\psi_{sf}=\psi_{sf}(L)} \tag{7.15}$$

and

$$g_m = \frac{W}{L}\mu_{nf}^*C_{of}[\psi_{sf}(L)-\psi_{sf}(0)] \tag{7.16}$$

If we assume that $\psi_{sf}(L)$ and $\psi_{sf}(0)$ are independent of V_{Gb} and V_B, then the back-gate transconductance g_{mGb} and body transconductance g_{mb} can be approximated as [93,95]

$$g_{mGb} = \frac{W}{L}\mu_{nf}^*C_{bb}[\psi_{sf}(L)-\psi_{sf}(0)] \tag{7.17}$$

and

$$g_{mb} = \frac{W}{L}\mu_{nf}^*C_b[\psi_{sf}(L)-\psi_{sf}(0)] \tag{7.18}$$

Using the assumptions $\psi_{sf}(L) \approx 2\phi_B + V_D$ and $\psi_{sf}(0) \approx 2\phi_B + V_S$ for a strongly inverted front-surface and the first approximation for I_{Df} in Chapter 6, we have C_{ij}' being given in Tables 1 and 2 of Lim and Fossum [87], and

$$g_{mGb}' = \frac{W}{L}\mu_{nf}^*C_{bb}V_{DS}, \tag{7.19}$$

and

$$g_{mb}' = \frac{W}{L}\mu_{nf}^*C_bV_{DS} \tag{7.20}$$

7.3 Results and Discussion

The small-signal parameters shown in Figs. 7.1 and 7.2 for a typical fully depleted SOI MOSFET with t_{of}=20 nm, t_{ob}=400 nm, t_f=200 nm, W=20 μm, L=10 μm, N_A=1×10^{16} cm^{-3}, and μ^*_{nf}=450 cm^2/V·sec under the assumptions $V^f_{FB} = V^b_{FB} = 0$, $V_S = 0$, and $V_B = 0$ for back surface accumulation have been evaluated over a wide range of V_{Gf} and V_{DS}. Figures 7.3 and 7.4 show the relation of eight capacitance coefficients in Fig. 7.1 versus front gate-source voltage ($V_{GfS} = V_{Gf}$ for $V_S = 0$) obtained from the numerical resolution of Eqs. (7.1)-(7.11) and the strong-inversion approximation in Eq. (7.19) for depleted back surface ($V_{Gb} = 0$). The three operation regimes are defined by [87]

$$V_{Gf} - V_{Tf} < 0 \longrightarrow Off, \tag{7.21}$$

$$0 \leq V_{Gf} - V_{Tf} \leq (1+\alpha)V_{DS} \longrightarrow Saturation, \tag{7.22}$$

and

$$V_{Gf} - V_{Tf} > (1+\alpha)V_{DS} \longrightarrow Linear \tag{7.23}$$

where $\alpha = C_{bb}/C_{of}$ and C_b/C_{of} for depleted and accumulated back surface, respectively. The threshold voltage V_{Tf} is given by

$$V^D_{Tf} = V^f_{FB} + (1+\alpha)2\phi_B - \alpha(V_{Gb} - V^b_{FB}) - \frac{(2C_b + C_{ob})Q_b}{2C_{of}(C_b + C_{ob})} \tag{7.24}$$

for back-surface depletion and

$$V^A_{Tf} = V^f_{FB} + (1+\alpha)2\phi_B - \frac{Q_b}{2C_{of}} \tag{7.25}$$

for back-surface accumulation. It should be noted that the parameters extracted from this model is valid for all regions of operation and no specific definition has been introduced for the off, saturation, and linear regimes. It is interesting to note that the calculated C_{gfs} as a function of V_{Gf} shown in Fig. 7.3 follows the same trend as the experimental results [98]. The dependence of the intrinsic capacitors on the drain-source voltage (V_{DS}) for the depleted back surface is shown in Figs. 7.5 and 7.6 respectively. By normalizing the capacitances in Fig. 7.5 to the front-gate oxide capacitance C_{of} ($=WLt_{of}/\epsilon_{ox}$ $\approx$0.34 pF), it is seen that the minimum value of C_{gfs}/C_{of} and the maximum value of C_{gfd}/C_{of} in the linear region are 0.5. Furthermore, value of C_{gfs}/C_{of} is about 2/3 in the saturation region [95]. Similarly, by using the normalizing factor C_{bb} ($\approx$14.7 fF) for the capacitances in Fig. 7.6, it yields 0.5 for minimum value of normalized C_{gbs} and maximum value of normalized C_{gbd} in the linear region, and approximately 2/3 for normalized C_{gbs} in the saturation region.

Figures 7.7-7.10 show the nine capacitance coefficients in Fig. 7.2 as a function of V_{Gf} and V_{DS} for accumulated back surface. These results are similar to those shown in Figs. 7.3-7.6 but the threshold voltage [from Eq. (7.26)] is shifted to the right. Since the back-surface potential is virtually pinned at zero for back-surface accumulation [77], the back gate-body capacitance of C_{gbb} is constant for all operation regions as expected. If the normalizing factor C_b ($\approx$0.103 pF) is employed for capacitances in Fig. 7.10, the results are in good agreement with simple theory [84], *i.e.*, the minimum value of C_{bs}/C_b and the maximum value of C_{bd}/C_b in the linear region are 0.5 while C_{bs}/C_b is about 2/3 in the saturation region. Although $C_{gfgb} \approx C_{gbgf}$ for depleted back surface and $C_{gfb} \approx C_{bgf}$ for accumulated back surface hold in the present model, the reciprocity ($C_{ij} = C_{ji}$) is not assumed for the capacitance coefficients in the equivalent circuits shown in Figs. 7.1 and 7.2.

The four conductance parameters shown in Figs. 7.1 and 7.2 are evaluated from Eqs. (7.15)-(7.18) as a function of V_{Gf}. The results are given in Fig. 7.11 for V_{DS}=1 V. Since C_{ob} is much smaller than C_{of} and C_b for a typical SOI MOSFET, value of g_{mgb} is expected to be much smaller than g_{mb} and g_m in the linear region.

7.4 Conclusion

By modifying the existing small-signal model for the bulk MOSFETs, a simple equivalent circuit for the fully depleted SOI MOSFETs has been presented. Under quasistatic operation, expressions for the parameters in the equivalent circuit have been derived by assuming a constant mobility and no short channel effects. The derived parameters are valid for all regions of operation. and no any assumptions to the regime of operation are necessary. The numerical simulations are in good agreement with the results derived from the first-order approximation using strong inversion theory [87].

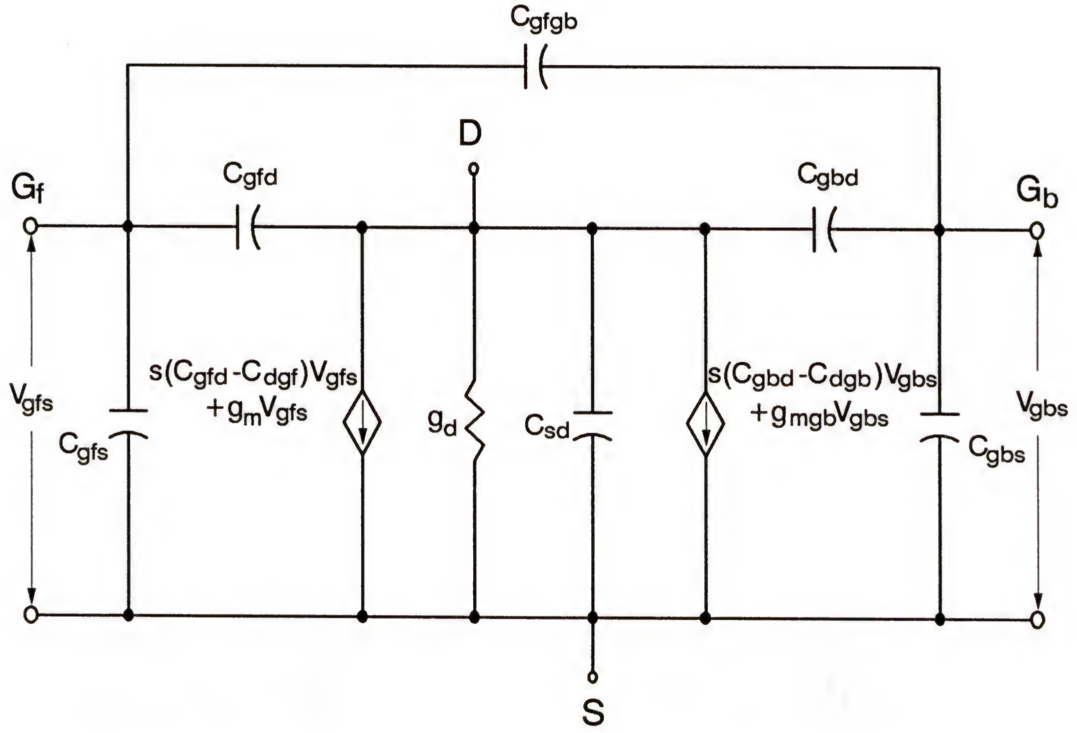


Figure 7.1 Small-signal equivalent circuit of a fully depleted SOI MOSFET for depleted back surface under quasistatic operation.

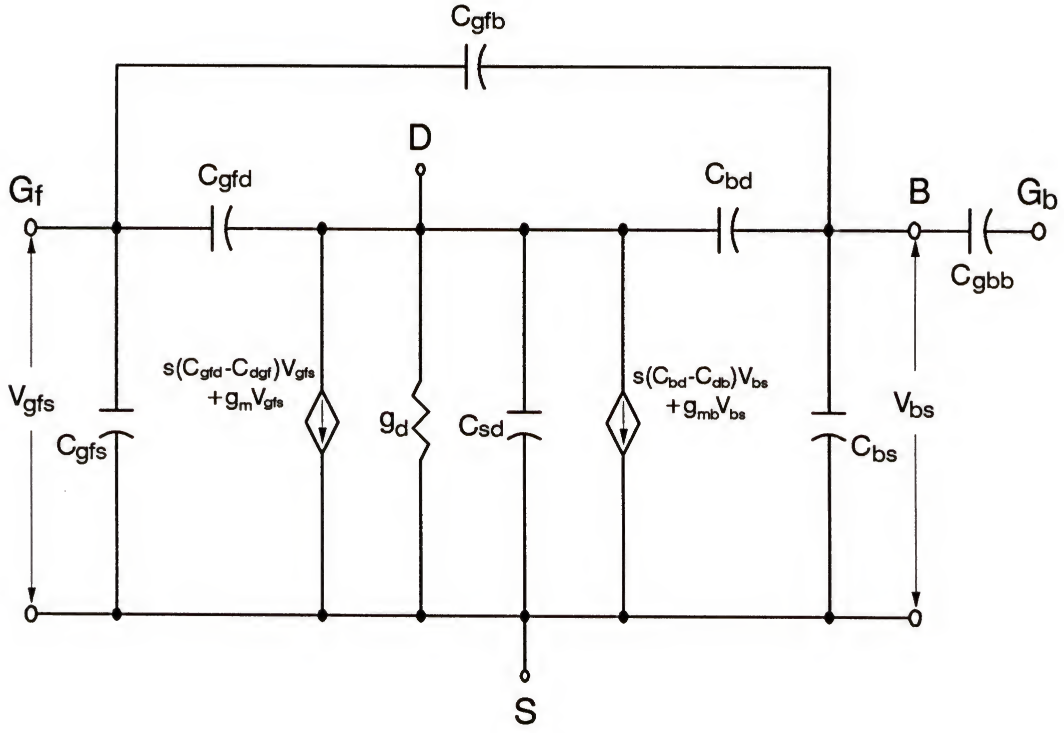


Figure 7.2 Small-signal equivalent circuit of a fully depleted SOI MOSFET for accumulated back surface under quasistatic operation.

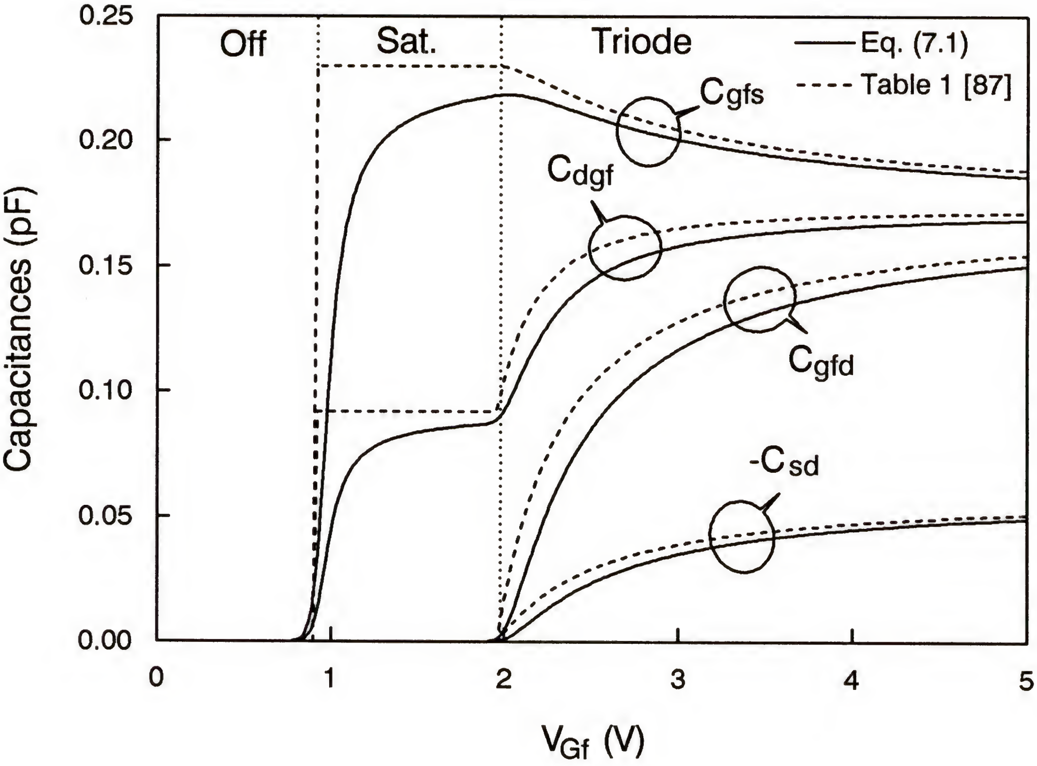


Figure 7.3 Capacitance coefficients C_{gfs}, C_{dgf}, C_{gfd}, and C_{sd} versus front gate-source potential V_{Gf} for depleted back surface (V_{Gb}=0 V) and V_{DS}=1 V. The strong-inversion approximation is obtained from Table 1 [87].

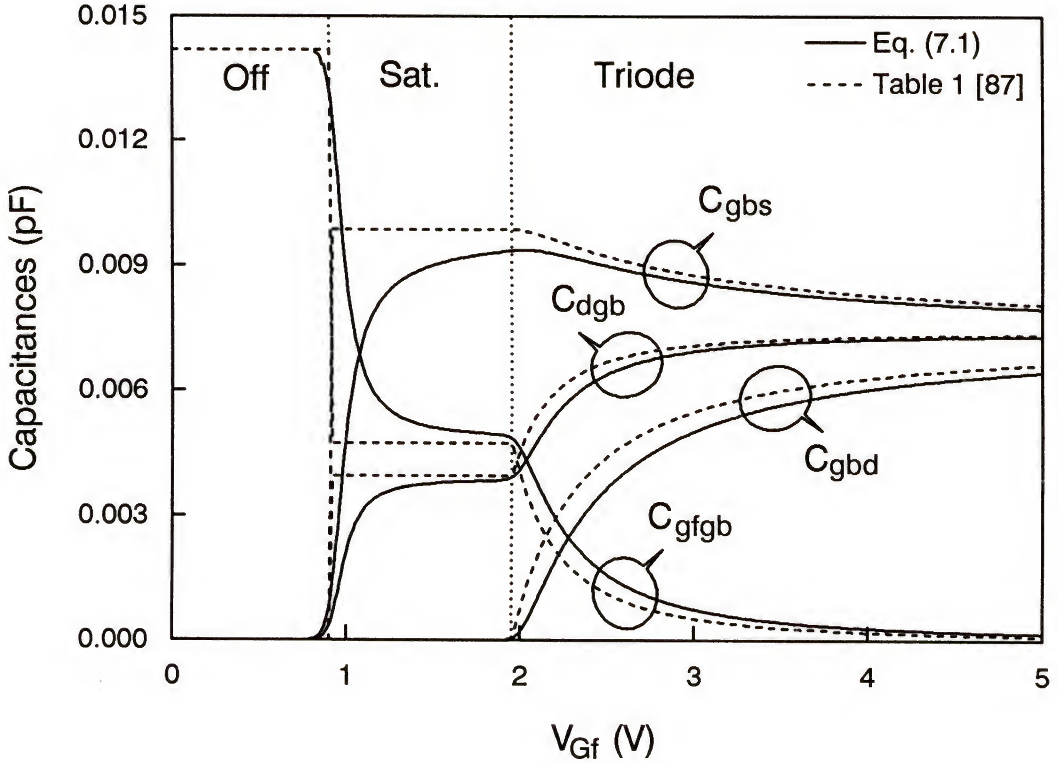


Figure 7.4 Capacitance coefficients C_{gbs}, C_{dgb}, C_{gbd}, and C_{gfgb} versus front gate-source potential V_{Gf} for depleted back surface (V_{Gb}=0 V) and V_{DS}=1 V. The strong-inversion approximation is obtained from Table 1 [87].

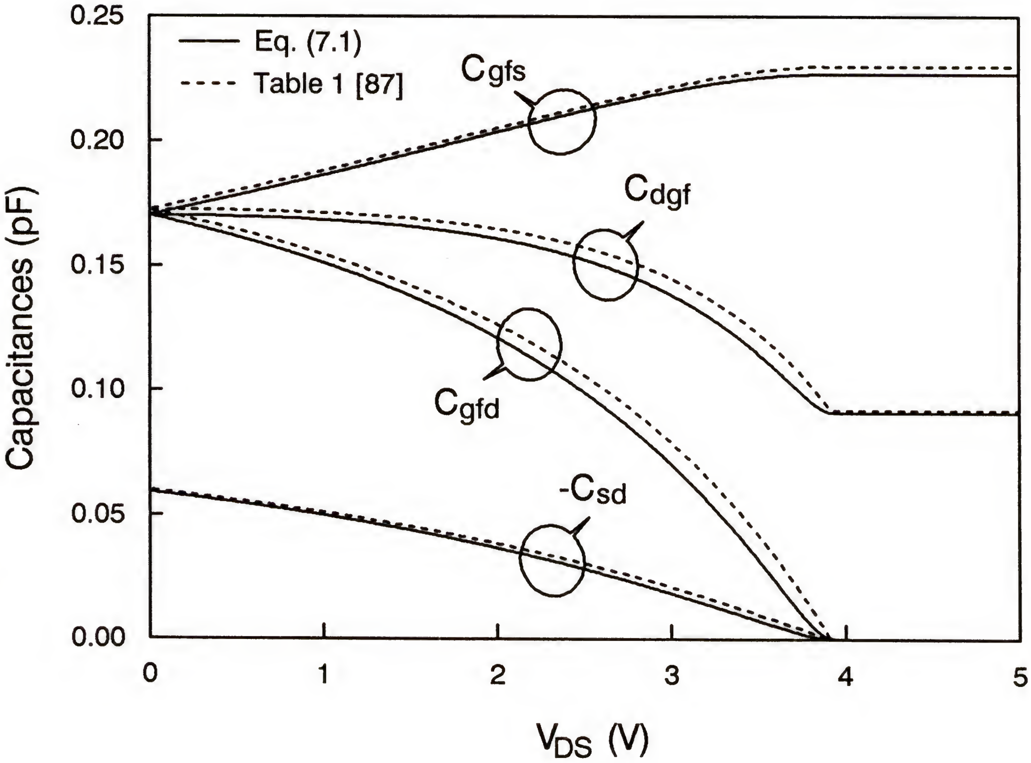


Figure 7.5 Capacitance coefficients C_{gfs}, C_{dgf}, C_{gfd}, and C_{sd} versus drain-source potential V_{DS} for depleted back surface (V_{Gb}=0 V) and V_{Gf}=5 V. The strong-inversion approximation is obtained from Table 1 [87].

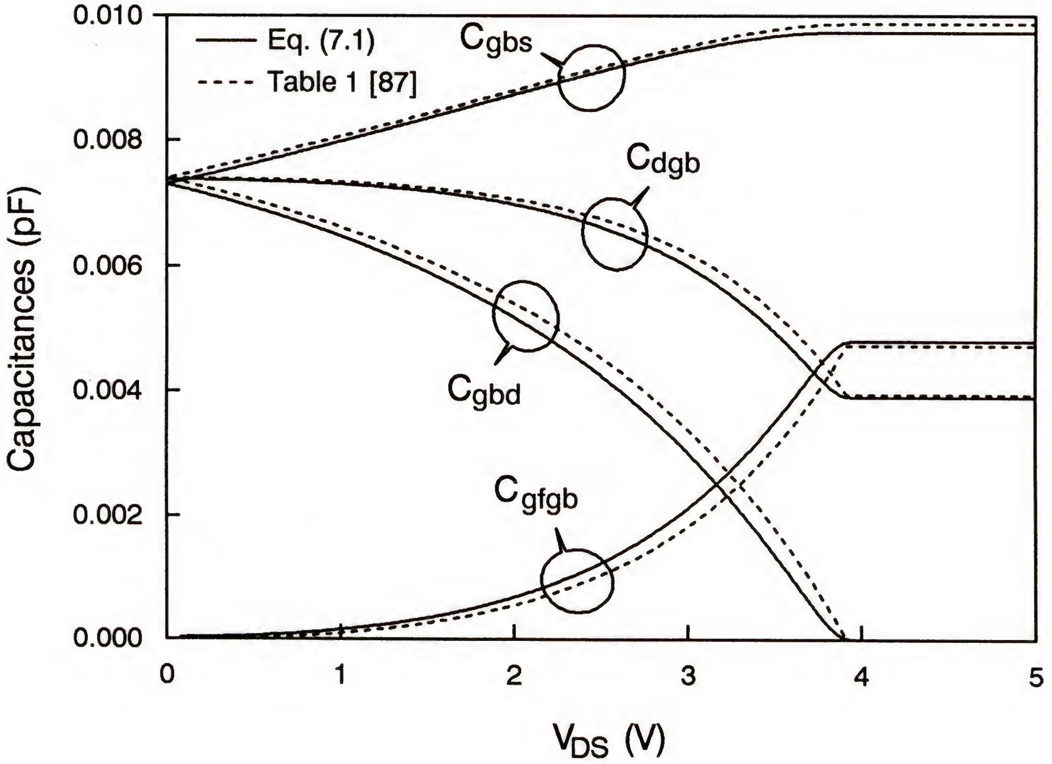


Figure 7.6 Capacitance coefficients C_{gbs}, C_{dgb}, C_{gbd}, and C_{gfgb} versus drain-source potential V_{DS} for depleted back surface (V_{Gb}=0 V) and V_{Gf}=5 V. The strong-inversion approximation is obtained from Table 1 [87].

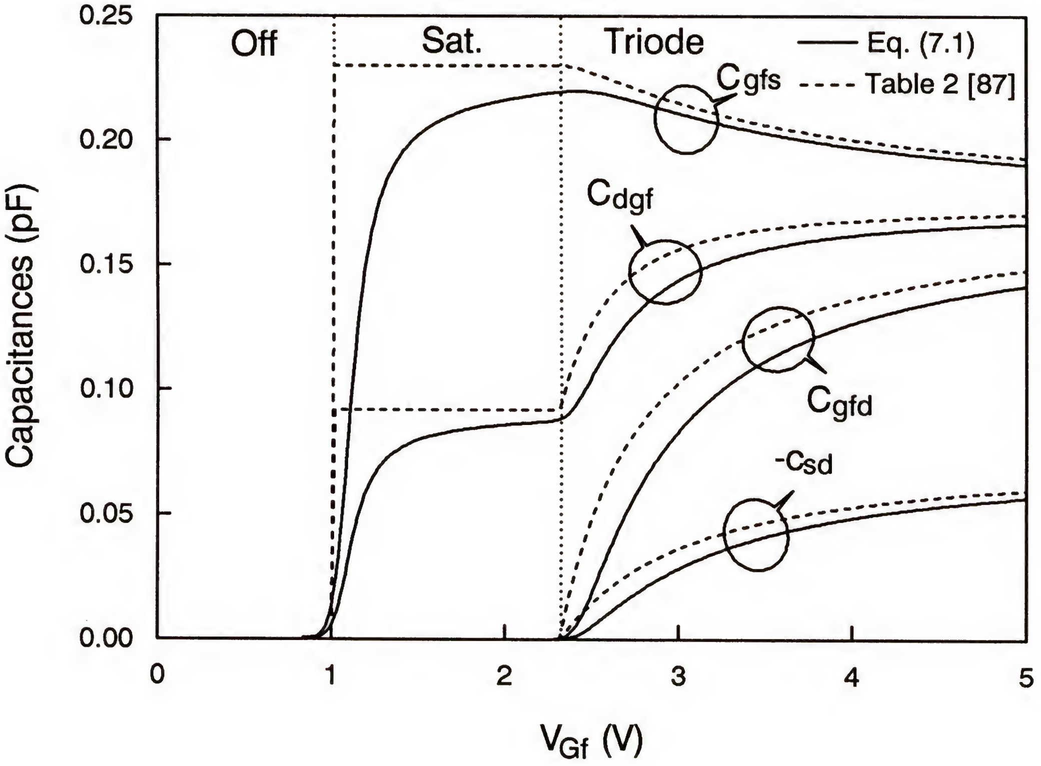


Figure 7.7 Capacitance coefficients C_{gfs}, C_{dgf}, C_{gfd}, and C_{sd} versus front gate-source potential V_{Gf} for accumulated back surface ($V_{Gb} = -20$ V) and V_{DS}=1 V. The strong-inversion approximation is obtained from Table 2 [87].

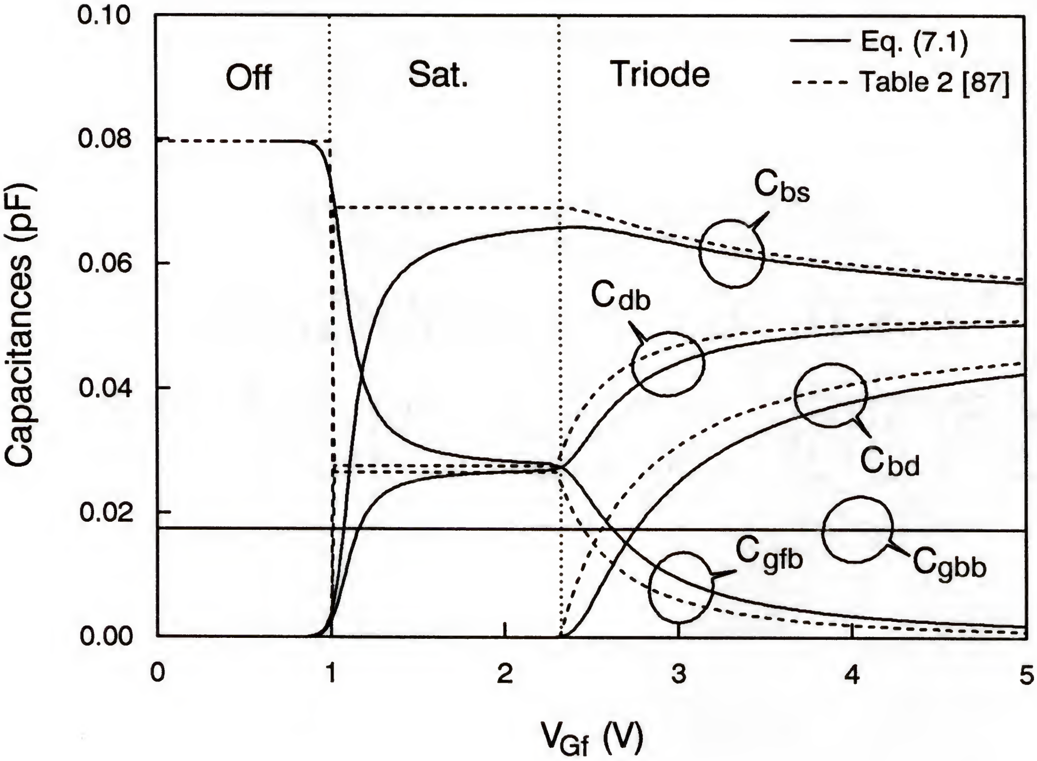


Figure 7.8 Capacitance coefficients C_{bs}, C_{db}, C_{bd}, C_{gfb}, and C_{gbb} versus front gate-source potential V_{Gf} for accumulated back surface ($V_{Gb} = -20$ V) and V_{DS}=1 V. The strong-inversion approximation is obtained from Table 2 [87].

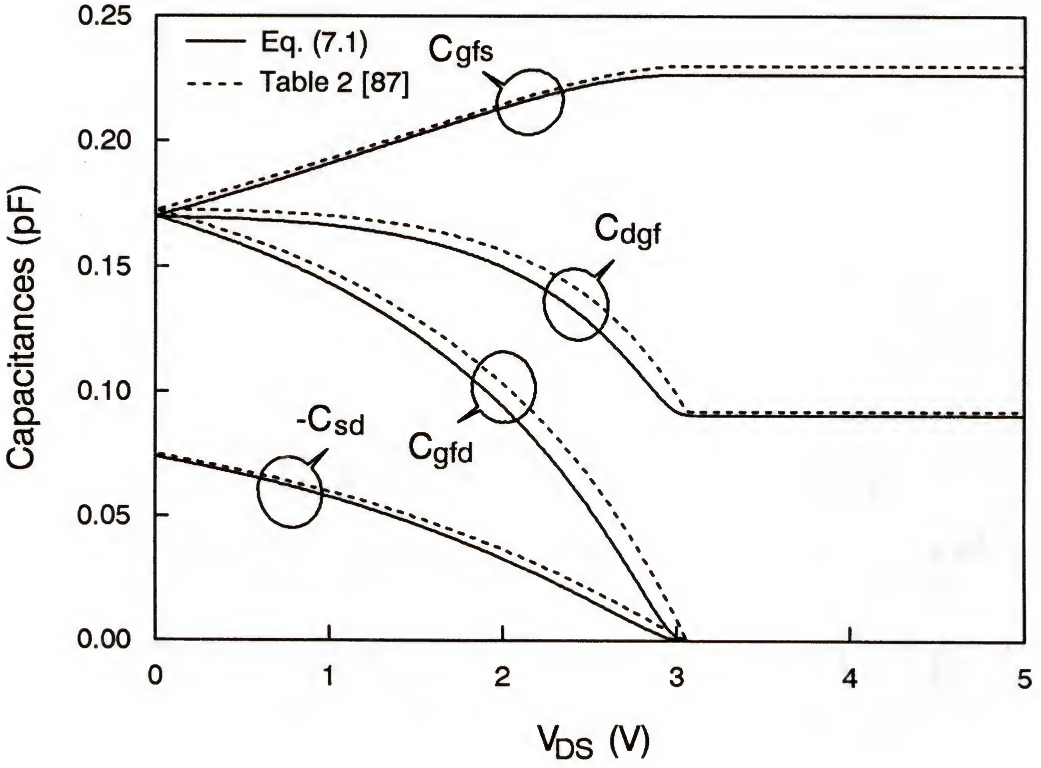


Figure 7.9 Capacitance coefficients C_{gfs}, C_{dgf}, C_{gfd}, and C_{sd} versus drain-source potential V_{DS} for accumulated back surface ($V_{Gb} = -20$ V) and V_{Gf}=5 V. The strong-inversion approximation is obtained from Table 2 [87].

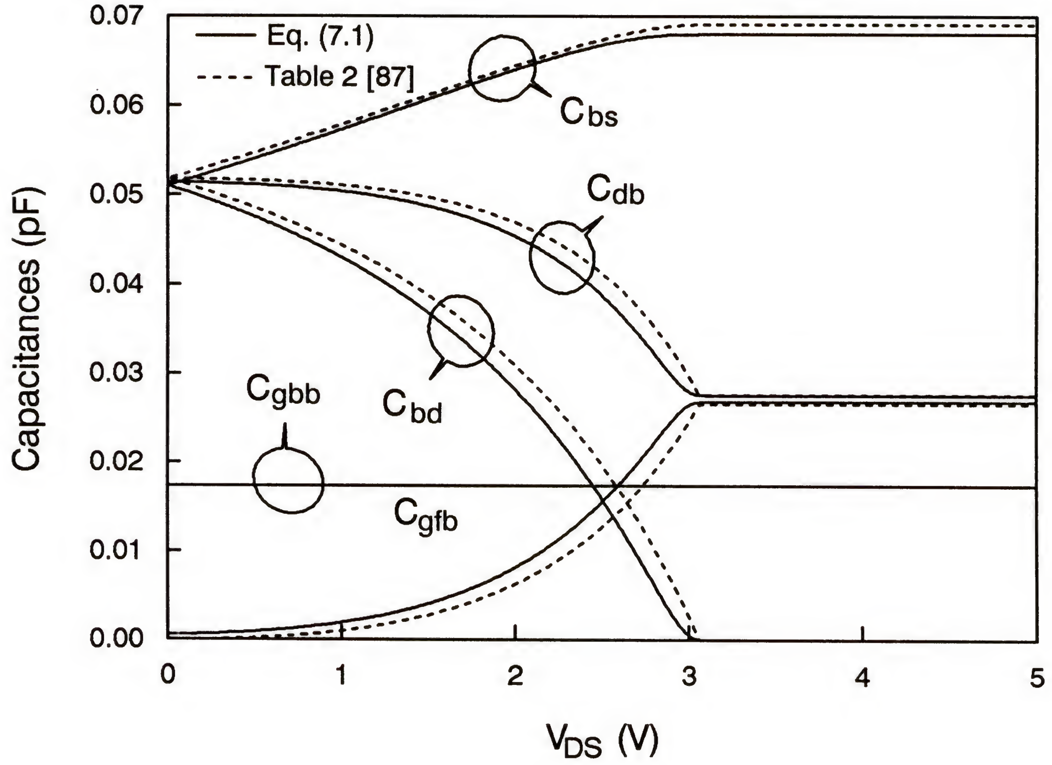


Figure 7.10 Capacitance coefficients C_{bs}, C_{db}, C_{bd}, C_{gfb}, and C_{gbb} versus drain-source potential V_{DS} for accumulated back surface ($V_{Gb} = -20$ V) and V_{Gf}=5 V. The strong-inversion approximation is obtained from Table 2 [87].

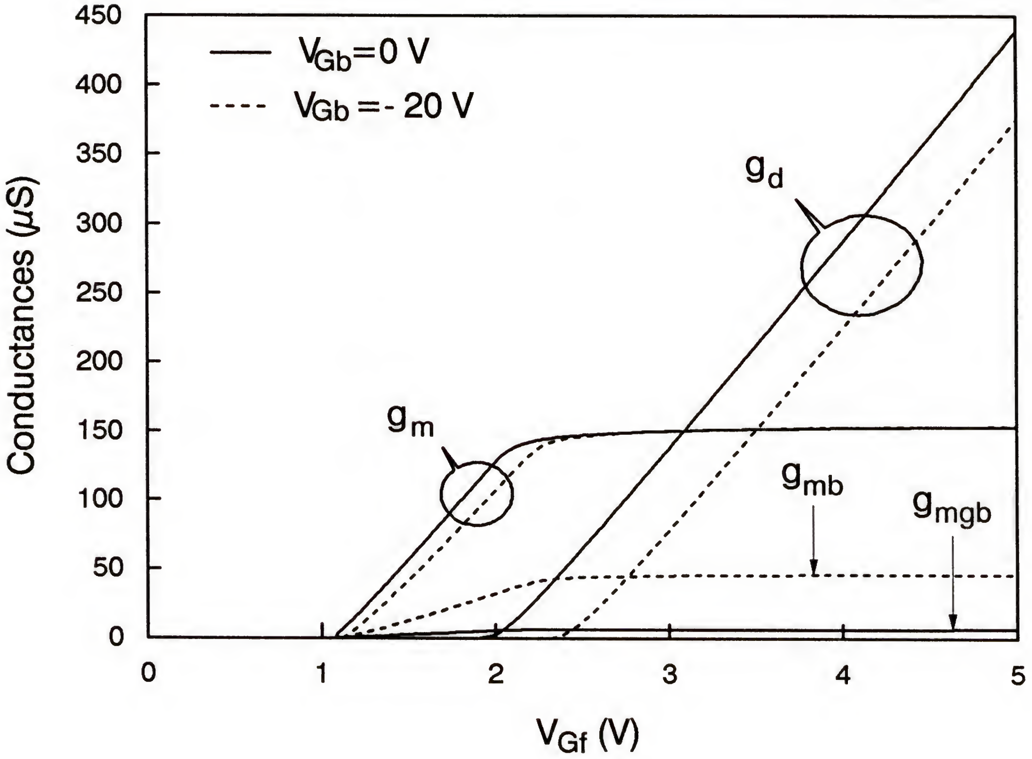


Figure 7.11 Conductance g_d [Eq. (7.15)], front-gate transconductance g_m [Eq. (7.16)], bulk transconductance g_{mb} [Eq. (7.18)], and back-gate transconductance g_{mgb} [Eq. (7.17)] versus front-gate voltage for V_{DS}=1 V with different back-gate voltages (V_{Gb}=0 V for depleted back surface and $V_{Gb} = -20$ V for accumulated back surface).

CHAPTER 8
SUMMARY AND CONCLUSIONS

The objective of this work is to develop new optical and electrical characterization techniques for analyzing the electrical and defect properties in ultra-thin SOI materials and devices. It consists of three parts. In the first part, a contactless dual-beam optical modulation technique for mapping and determination of film and substrate carrier lifetimes in SOI wafers has been developed for evaluating the quality of incoming wafer lots to avoid fabricating VLSI circuits on poor quality SOI materials. A theoretical model is developed to extract the excess carrier lifetimes in the SIMOX film and substrate by the DBOM technique. In the second part, two electrical characterization techniques using test structures of thick- and thin-film SOI MOSFETs for determining the interface properties of the SOI devices have been developed. In the third part, analysis of current-voltage characteristics and extraction of small-signal parameters for fully depleted SOI MOSFETs has been carried out.

The film and substrate carrier lifetimes in SIMOX wafers can be determined by using a contactless DBOM technique. The DBOM method is based on the modulation of the transmission intensity of an infrared (IR) probe-beam by a visible pump-beam ($h\nu \geq E_g$) via free carrier absorption in the SIMOX wafer. A theoretical model has been developed for extracting the excess carrier lifetimes in both the film and substrate of the SOI wafer by using the DBOM technique. It has been found that the uniformity of the excess carrier lifetimes in the film and the substrate will increase with increasing film thickness, and was more uniform in the center region than near the edge of the wafer. This method is particularly useful for monitoring the contamination and mapping the film carrier lifetimes profile in the starting SOI wafers. The rseults showed that film excess carrier lifetimes were one to two orders of magnitude smaller than the substrate carrier lifetimes for the SIMOX wafers studied in this work.

Interface states characterization in SOI MOSFETs is a subject of intensive research in recent years. Due to the complex multi-interface nature, small film thickness, and samll gate area of the SOI MOSFETs for VLSI circuit applications [96,99,100], it is difficult to determine the interface state properties by using the charge pumping or conventional capacitance and conductance methods. The modified high-low-frequency transconductance method has been successfully applied to characterize the properties of film/front-gate-oxide and film/buried-oxide interfaces of partially and fully depleted SOI MOSFETs operating in linear region. By comparing the real part of the measured high- and low-frequency transconductance and using a static drain current to gate voltage measurement, the energy distribution of the interface state density is determined without knowing the doping profile in the channel. The measured front-gate interface state density at midgap for the multi-oxygen implanted (MI) substrate is almost the same as that of a bulk MOSFET, and is lower than that of the single-oxygen implanted (SI) substrate. For a fully depleted MOSFET, the back-gate interface state density was found to be higher than that of the front gate.

Since the threshold voltage of a fully depleted SOI MOSFETs is sensitive to the interface states and gate bias, it is possible to determine the interface state density profile from the threshold voltage measurements. A new threshold voltage method for characterizing the interfcae state densities profile in thin (fully depleted) film SOI MOSFETs has been developed in this work. This technique is particularly attractive since it requires only simple static drain current measurements. The interface state density profiles obtained by this technique is similar to that by the HLF method.

Current-voltage characteristics for fully depleted SOI MOSFETs has been analyzed by relating the inversion charge density to the front surface potential from the theories developed for the bulk and SOI MOSFETs. This analysis, which is valid for back surface depletion and accumulation, describes correctly the threshold voltage, the drain current, and the transconductance in all regions of operation. The charge-sheet model and strong-inversion assumption are used in the analysis. The charge-sheet model was found to be a good approximation for the SOI MOSFETs.

In the analog MOS circuit design, it is necessary to derive a small-signal model for SOI MODFETs. By making simple revision to the existing models for the bulk MOSFETs, a small-signal equivalent circuit model is developed for the SOI MOSFETs. Based on the charge-neutrality relation and current-voltage characteristics under quasistatic operation, the small-signal parameters are extracted for thin-film SOI MOSFETs in all regions of operation from the relationships between the free carrier charge density, surface potential, applied drain voltage, and the applied front- and back-gate voltages. The short-channel effects [14,15,88] are neglected in the present analysis for simplicity in the extraction of small-signal parameters and analyzing the current-voltage characteristics.

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APPENDIX 1

From the gradual channel approximation and charge-sheet model, the drain current for an n-channel SOI MOSFET is given by

$$I_{Df} = -W\mu_{nf}^{*}\left[Q_{nf}(d\psi_{sf}/dy) - \frac{1}{\beta}(dQ_{nf}/dy)\right] \tag{A.1}$$

The derivatve dQ_{nf}/dy can be obtained from Eq. (6.6) as

$$dQ_{nf}/dy = (1 + \delta C_b/C_{of})(d\psi_{sf}/dy) \tag{A.2}$$

Substitution of Eq. (A.2) into Eq. (A.1) gives

$$I_{Df} = -W\mu_{nf}^{*}[Q_{nf} - (C_{of}/\beta)(1 + \delta C_b/C_{of})]\frac{d\psi_{sf}}{dy} \tag{A.3}$$

which is equivalent to Eq. (6.18).

APPENDIX 2

The current ΔI^D_{Df} in Eq. (6.30) for depleted back surface can be expressed as

$$\begin{aligned}\Delta I^D_{Df} = \frac{W}{L}\mu^*_{nf}C_{of}\frac{1}{\beta}\Bigg\{&\left(1+\frac{C_{bb}}{C_{of}}\right)[\psi_{sf}(L)-\psi_{sf}(0)]+\frac{2}{C_{of}}(C-D)\\ &+\frac{2}{B^{1/2}}\left(V_y+\frac{\lambda^2 C_{fbb}}{C_b}+\frac{C_b}{\lambda^2 C_{of}^2 C_{fbb}}A\right) ln\left[\frac{(C-s_1)(D-s_2)}{(C-s_2)(D-s_1)}\right]\\ &+\frac{2\lambda^2 C_{fbb}}{C_b} ln\left[\frac{(C-s_1)(C-s_2)}{(D-s_1)(D-s_2)}\right]\Bigg\}\end{aligned} \tag{B.1}$$

where $C_{fbb}^{-1} = C_{of}^{-1} + C_b^{-1} + C_{ob}^{-1}$,

$$A = -\frac{\lambda^2 C_{of}^2 C_{ob}}{C_{ob}+C_b}\left(V_{Gb}-V_{FB}^b+\frac{Q_b}{2C_{ob}}\right), \tag{B.2}$$

$$B = 1+\frac{C_b}{\lambda^2 C_{of} C_{fbb}}\left(C_{of}V_y+\frac{C_b}{\lambda^2 C_{of} C_{fbb}}A\right), \tag{B.3}$$

$$C = \left(A+\frac{\lambda^2 C_{of}^2 C_{ob}}{C_{ob}+C_b}\psi_{sf}(L)\right)^{1/2}, \tag{B.4}$$

$$D = \left(A+\frac{\lambda^2 C_{of}^2 C_{ob}}{C_{ob}+C_b}\psi_{sf}(0)\right)^{1/2}, \tag{B.5}$$

$$s_1 = \frac{\lambda^2 C_{of} C_{fbb}(1+B^{1/2})}{C_b}, \tag{B.6}$$

$$s_2 = \frac{\lambda^2 C_{of} C_{fbb}(1-B^{1/2})}{C_b}, \tag{B.7}$$

and V_y is given in Eq. (6.32). For accumulated back surface, the current ΔI^A_{Df} in Eq. (6.42) is given by

$$\begin{aligned}\Delta I^A_{Df} = \frac{W}{L}\mu^*_{nf}C_{of}\frac{1}{\beta}\Bigg\{&\left(1+\frac{C_b}{C_{of}}\right)[\psi_{sf}(L)-\psi_{sf}(0)]+2\lambda[\psi_{sf}^{1/2}(L)-\psi_{sf}^{1/2}(0)]\\ &+\frac{2\lambda C_{of}}{K}\left(V_z+\frac{\lambda^2 C_{of}}{C_{of}+C_b}\right) ln\left[\frac{(\psi_{sf}^{1/2}(L)-s_3)(\psi_{sf}^{1/2}(0)-s_4)}{(\psi_{sf}^{1/2}(L)-s_4)(\psi_{sf}^{1/2}(0)-s_3)}\right]\end{aligned}$$

$$+\frac{2\lambda^2 C_{of}}{C_{of}+C_b} ln \left[\frac{(\psi_{sf}^{1/2}(L) - s_3)(\psi_{sf}^{1/2}(L) - s_4)}{(\psi_{sf}^{1/2}(0) - s_3)(\psi_{sf}^{1/2}(0) - s_4)} \right] \Bigg\} \tag{B.8}$$

where

$$K = [\lambda^2 C_{of}^2 + V_z C_{of}(C_{of} + C_b)]^{1/2}, \tag{B.9}$$

$$s_3 = \frac{\lambda C_{of} + K}{C_{of} + C_b}, \tag{B.10}$$

$$s_4 = \frac{\lambda C_{of} - K}{C_{of} + C_b}, \tag{B.11}$$

and V_z is given in Eq. (6.44).

BIOGRAPHICAL SKETCH

Ping-Chang Yang was born in Kaohsiung, Taiwan, R.O.C., on December 16, 1962. He received the B.S. degree in the Department of Electronics Engineering and M.S. degree in the Graduate Institute of Electronics from the National Chiao Tung University in 1985 and 1987, respectively.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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